Formation and Characterization of SrBi$_2$Ta$_2$O$_9$ (SBT) Thin Film Capacitor Module with Platinum/Titanium Bottom and Platinum Top Electrodes

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gorgelegt von

Diplom-Physiker Univ.
Walter Hartner
aus Lauingen / Donau

Berichter: Univ.-Prof. Dr.-Ing. Rainer Waser
Univ.-Prof. Dr.rer.nat. Klaus Heime

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1. Introduction

Many companies have pursued the dream of the perfect memory. The specifications are universally known: non-volatile, fast to read, fast to write, bit erasable, electrically re-programmable, low power, durable, dense and cheap [Ele97]. There are DRAM, SRAM, EPROM and Flash. However, it takes all sorts to make up the memory world and none of them is perfect. But FeRAM (Ferroelectric Random Access Memory) could be.

Although it was known since the discovery of the ferroelectricity in 1921 that the polarization states could be used as the binary digits for storing information, the effort of the chip manufacturer to develop and to use ferroelectric materials in semiconductor memories did not happen until very recently. The main driver for this emerging technology was the DRAM business. The DRAM architecture is the simple one transistor / one capacitor cell (1T/1C cell). The capacitors in DRAMs usually have nitride and oxide layers (NO) as dielectric [Maz98]. The dielectric constant for this insulator is in the order of 6. To enhance the memory cell capacitance for higher memory densities as feature sizes decrease, dielectric thickness reduction, hemispherical polysilicon, fins stack and crowns (for stack capacitors), and deep trenches for area enlargement have been introduced [Bal99]. However, every major DRAM manufacturers realized at the beginning of the 90’s that the additional process steps are approaching their practical limits to maintain the cell capacitance with the NO dielectric. Therefore, new upcoming DRAM generations will require materials with higher values for the dielectric constant $k$ or $\varepsilon_r$ [Faz94] [Ish93]. Ferroelectrics with the Curie point around the operation temperature of the memory (usually room temperature - RT) have large dielectric constants. One of the most promising materials for high-$k$ DRAMs is $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST) [Hön99] [Bei99]. Now the semiconductor industry was open to investigate new ferroelectric materials and electrodes even in a standard semiconductor production line. Since the basic issues for both high-$k$ DRAM and NV-FeRAM (Non-Volatile FeRAM) are very similar, every major DRAM manufacturer installed projects for developing high density FeRAMs [Sie99]. The first semiconductor company which succeeded in making low density solid state ferroelectric memory devices (a few KB) with PbZr$_{1-x}$Ti$_x$O$_3$ (PZT) was Ramtron International Corporation [Phi96]. Besides the well-known PZT, the newer bismuth layered perovskite $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) are promising ferroelectric materials for the use in FeRAMs [Auc98] [Ara95] [Ara96]. Ramtron International Corp. and Symetrixx Corp., Colorado Springs USA patent uses of PZT and SBT for thin film FeRAM fabrication, respectively.

In a DRAM, the dielectric is not ideal, but contains defects and impurities that make the capacitor leaky. The loss of charge means that the stored information will disappear with time. In order to keep the information and to separate the binary digits "1" and "0", the charge of the capacitor has to be read and rewritten on a permanent basis. This is called a refresh and has to be done every 10-30 ms in a DRAM, depending on the quality of the dielectric. If the power is switched off, all information that has not been
saved is lost. In a nonvolatile memory this problem does not exist. Existing nonvolatile memories like EPROM (Erasable Programmable), EEPROM (Electrically Erasable Programmable) and Flash EPROM suffer from high voltage writing (12-16V), slow writing times in the ms range and from deterioration in memory function after $\sim 10^6$ write cycles. When comparing properties of DRAM, Flash, SRAM and FeRAM, FeRAMs offer the possibility of an universal RAM (see table 1). Especially interesting for mobile applications are FeRAMs with SBT due to their low voltage/low power behavior. Due to these properties, high densities FeRAMs (>1Mb) provide enormous business potential. Low density FeRAMs (kb range) are already in production by Ramtron [Phi96], Matsushita [Sum95] [Fuj97b] and Fujitsu [Ito00].

<table>
<thead>
<tr>
<th>FeRAM</th>
<th>DRAM</th>
<th>FLASH</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>read cycles</td>
<td>$10^{10}$-$10^{12}$-$10^{15}$</td>
<td>$10^{15}$</td>
<td>$10^{15}$</td>
</tr>
<tr>
<td>write cycles</td>
<td>$10^{10}$-$10^{12}$-$10^{15}$</td>
<td>$10^{15}$</td>
<td>$10^6$</td>
</tr>
<tr>
<td>write voltage</td>
<td>5V --&gt; 0.8V</td>
<td>1.0 - 5V</td>
<td>12 - 16V</td>
</tr>
<tr>
<td>access time</td>
<td>&lt; 100ns --&gt; 20ns</td>
<td>40 - 70ns</td>
<td>40 - 70ns</td>
</tr>
<tr>
<td>write time</td>
<td>&lt; 100ns --&gt; ns</td>
<td>ns</td>
<td>$\mu$s - ms</td>
</tr>
<tr>
<td>cell size</td>
<td>1x</td>
<td>1x</td>
<td>1x</td>
</tr>
<tr>
<td>data retention (power off)</td>
<td>&gt;10 years</td>
<td>no</td>
<td>&gt; 10 years</td>
</tr>
</tbody>
</table>

Table 1: Properties of different memory types. For FeRAM, see on the left side properties of currently available FeRAMs, and on the right side values for optimized devices [Deh99].

Although standard CMOS processes can be used for frontend and backend processes, FeRAM technology development has to overcome major challenges due to new materials used for capacitor formation. This work investigates and characterizes SrBi$_2$Ta$_2$O$_9$ (SBT) thin film capacitor processing and its impact on electrical and physical behavior using Pt as electrode material. Pt is the electrode material of choice due to its chemical inertness. SBT was coated using metal organic deposition (MOD). The interaction of Pt and SBT during processes like annealing and etching is not only crucial for the understanding of the process itself but also for the performance of the capacitor. This interaction between electrode and ferroelectric layer gets even more important when ultra thin ferroelectric layers and deep sub micron features are considered. Each step in the formation of a ferroelectric capacitor has its own specific impact on the performance of the device. The objective of the thesis is to analyze these influences and interactions of the Pt/SBT/Pt layer stack during bottom electrode processing, SBT layer annealing, top electrode patterning and hydrogen annealing.
The thesis is presented in six chapters. After this introduction, the basic concepts of ferroelectricity and FeRAM’s are outlined in chapter 2. Here the reader will find besides the basic definitions for ferroelectricity and FeRAM’s, a summary about the SBT material. An overview about the challenges in integration of ferroelectric thin films into a IC device and a comparison of the main integration concepts are also given in chapter 2. Chapter 3 deals with the experimental techniques which were used for this thesis. In chapter 3 the characterization and measurement methods as well as the processes for the ferroelectric capacitor formation will be reviewed. The main results of this work are given in the remaining chapters. The sequence of these chapters follows the process flow of building a ferroelectric capacitor (bottom electrode, ferroelectric layer, top electrode, patterning and influence of the backend processes like the hydrogen rich forming gas anneal).

In chapter 4 the effects of the Pt/Ti bottom electrode on microstructural and electrical properties of SBT thin films will be investigated. In Chapter 5 the SBT layer processing with its different thermal treatments and its influence on grain growth will be studied. After SBT layer and top electrode processing the capacitor have to be patterned. The emphasis, therefore, in chapter 6 is placed on electrical results and degradation mechanism of Pt/SBT/Pt capacitors after etching. The degradation mechanisms of SBT thin film capacitors in a hydrogen ambience is presented in chapter 7. Finally, chapter 8 presents a summary and conclusions about processing SBT thin film capacitor with Pt/Ti bottom and Pt top electrodes.
2. Ferroelectricity and FeRAM

2.1. Basis Concepts of Ferroelectricity

The function of the FeRAM is based on the remanent polarization of the ferroelectric material. Therefore, this chapter will give a brief description about the physical mechanisms that give rise to the remanent polarization in ferroelectric materials. The degree of remanent polarization depends on microscopic mechanisms that also takes place in dielectric materials. In order to understand the mechanisms that cause remanent polarization in ferroelectric materials, the basic properties of dielectric materials are summarized. More information about dielectrics and ferroelectrics can be found in [Xu91] and [Kit96].

Dielectric materials

Due to strong bonds between valence electrons and atoms, dielectrics are good electric insulators. Dielectrics are found in covalent and ionic bound materials, such as polymers, glasses and ceramics. Even though these materials are poor conductors, they are not inert to an external electric field. The field causes a distortion of the charge balance within the material. Between the negative and positive charge center a dipole is formed. This is the source for the term dielectric. The dipole moment \( p \), for two opposite point charges is defined as

\[
\vec{p} = \vec{Q} \cdot \vec{l}
\]  
[eq. 1]

where \( \vec{Q} \) is the charge magnitude of each point charge and \( \vec{l} \) is the spatial vector from the negative to the positive point charge. Polarization \( \vec{P} \) is defined as the dipole distribution over a volume

\[
\vec{P} = \frac{d\vec{p}}{dV}
\]  
[eq. 2]

and given in units of C/m². The polarization can also be expressed as

\[
\vec{P} = (\varepsilon_r - 1)\varepsilon_0\vec{E} = \varepsilon_r\varepsilon_0\vec{E}
\]  
[eq. 3]

where \( \varepsilon_r \) is the relative dielectric permittivity, \( \varepsilon_0 \) is the permittivity of free space and \( \chi \) is the dielectric susceptibility. The slope of the polarization curve gives the relative dielectric constant \( \varepsilon_r \) (see Figure 1a with linear and non-linear materials). In contrast to linear dielectrics, for non-linear dielectrics like ferroelectric materials, two types of permittivity can be defined, namely small-signal and differential permittivity. The former is defined only for electronic and non-switching polarization’s at \( E \rightarrow 0 \) or \( E \ll E_c \), and the differential permittivity is defined also by inelastic polarization as the slope of the hysteresis loop at any point. In Figure 1b the different behavior in \( C(V) \) measurements for linear and non-linear materials is also shown.
The polarization is composed of several components that can be divided in displacive and orientation polarization [Kit96].

(i) **Electronic polarization** occurs in all dielectric materials. Under an applied electric field the electrons are displaced very slightly towards the positive electrode and the nucleus very slightly towards the negative electrode. As soon as the external electric field is removed, the electrons and nucleus return to their original states and the induced dipoles disappear. Due to the very small separation between the positive and negative charge centers, the total amount of polarization is small compared with the other mechanisms of polarization.

Figure 1: (a) Polarization versus applied field for linear and non-linear materials. The slope of the curve gives the relative dielectric constant $\varepsilon_r$. (b) C(V) curves for linear and non-linear materials.

(ii) **Space charge polarization** results from charge defects caused by radiation, thermal deterioration or from the fabrication process. For example these can be stacking faults in the crystal, vacant sites, grain boundaries etc. between the charged defects form permanent dipoles. At zero electric field the charged defects are randomly distributed in the material. Under an external field the positively and negatively charged defects separate, which in turn causes a macroscopic polarization.

(iii) **Atomic and ionic polarization** involves the displacement of atoms and ions within the crystal structure under an applied electric field. A wide range of polarization effects is possible through this mechanism. Atomic or ionic polarization depend on crystal structure, solid solution of contaminants etc.

(iv) **Orientation polarization** involves reorientation of permanent dipoles. At zero electric field the permanent dipoles are randomly distributed. Under an external electric field they align with the direction of the field, so that the negative side faces the positive electrode and vice versa. The large separation
between the charge centers in permanent dipoles results in a much higher degree of polarization than for example electronic polarization.

**Ferroelectricity**
A ferroelectric material is a non-linear dielectric that exhibits a remanent polarization in the absence of an external electric field. Valasek discovered ferroelectricity in 1921 in Rochelle salt. Although the first syllable of the name suggests that ferroelectricity has something to do with iron, ferroelectric materials do not. The name ferroelectricity comes from the similarities between polarization of ferroelectric materials with magnetization of ferromagnetic materials. In a ferroelectric material a transition occurs from a centro-symmetric to a non-centro-symmetric unit cell at the Curie point $\Theta_c$. The shift in structural symmetry affects both structural and physical properties of the crystal.

Figure 2: (a) The potentials allow the cations in a unit cell to oscillate. Left with center of symmetry and right without center of symmetry [Xu91]. (b) The unit cell of the perovskite structure $A^{4+}B^{2+}O_3$ like PZT [Phi96].

After the transition the symmetry of the unit cell is disturbed so that several stable off-center positions are formed (Figure 2a,b). The Coulomb interactions between the cations in these off center positions and its coordinating anions do not cancel, which means that the unit cell possesses a permanent polarization. The two different states shown in Figure 2 represent the two logic states “0” and “1” in a memory.

In ferroelectrics, the temperature dependence of the dielectric constant above the Curie point (in the paraelectric phase regime) can be described fairly accurately by the Curie-Weiss law

$$\varepsilon = \varepsilon_o + \frac{C}{\Theta - \Theta_o}$$

where $C$ is the Curie-Weiss constant and $\Theta_o$ the Curie-Weiss temperature. $\Theta_o$ is different from the Curie point $\Theta_c$. $\Theta_o$ is a formula constant obtained by extrapolation, while $\Theta_c$ is the actual temperature where the
crystal structure changes. In the case of first-order phase transition $\Theta_0 < \Theta_c$, while for second-order phase transition $\Theta_0 = \Theta_c$ (Figure 3).

Based on the phase transition theory of Landau-Ginzburg, Devonshire developed a phenomenological theory of ferroelectricity by choosing the polarization $P$ and the temperature $\Theta$ as an order parameter [Xu91]. Since the Gibbs free energy $G$ is not changed by reversing the direction of the axes of the space coordinate system and is independent of the direction of the polarization $P$, $G$ can be expressed in an even power series of polarization

$$G(P, \Theta) = G_0(\Theta) + \frac{1}{2} \beta(\Theta) P^2 + \frac{1}{4} \xi(\Theta) P^4 + \frac{1}{6} \zeta(\Theta) P^6 + ...$$  \hspace{1cm} [eq. 5]

where $G_0$ is the elastic Gibbs free energy of the system when $P=0$ and the coefficients $\beta, \xi, \zeta, ...$ are functions of temperature.

Figure 3: (a) Functional relations of $\chi^{-1}(\Theta)$ and $P(\Theta)$ near the first order phase transition. $\Theta$ is the temperature with $\Theta_0$ being the Curie-Weiss temperature and $\Theta_c$ being the Curie point. (b) Functional relations of $\chi^{-1}(\Theta)$ and $P(\Theta)$ near the second order phase transition [Xu91].
A stable state of the thermodynamic system is characterized by a minimum value of the free energy $G$. The conditions for a minimum of $G$ are

$$\frac{\partial G}{\partial P} = 0; \quad \frac{\partial^2 G}{\partial P^2} = \chi^{-1} > 0$$

[eq. 6]

The equation of state for the ferroelectric system then takes the form

$$P\left(\beta(\Theta) + \xi(\Theta)P^2 + \zeta(\Theta)P^4\right) = 0 \text{ with } \xi^{-1}(\Theta) - 4\beta(\Theta)\zeta(\Theta) > 0$$

[eq. 7]

$$\beta(\Theta) + \xi(\Theta)P^2 + 5\zeta(\Theta)P^4 > 0$$

[eq. 8]

Two roots can be found for the left side of [eq. 7]. The first root $P=0$ corresponds to a paraelectric phase and the second root $P \neq 0$ to a ferroelectric phase. In the case of $P \neq 0$, one result of [eq. 7] and [eq. 8] corresponds to a first-order phase transition when $\xi < 0$ (Figure 3a), and the other result corresponds to a second-order phase transition when $\xi > 0$ (Figure 3b) [Xu91].

A typical phenomena seen in ferroelectrics is the formation of ferroelectric domains due to the minimization of the elastic and electrostatic energies in the crystal (Figure 4). The transformation is associated with an elongation in the direction of polarization. In order to minimize the elastic energy at grain boundaries and/or defects, the crystal divides itself into twinning domains that results in the same grain shape as before the transformation (Figure 4a). The other explanation is that domains are formed in order to minimize the electrostatic forces that act on the crystal faces due to the spontaneous polarization from the transition (Figure 4b). As the film gets thinner or the grain smaller, domains are formed in order to minimize the elastic and electrostatic forces compensated by strain relief.

![Figure 4: The two mechanisms supposed to be the reason for domain formation in ferroelectric crystals. The minimization of elastic (a) and electrostatic energy (b) [Was98].](image)

A ferroelectric crystal has always a multiple domain structure after that it has been grown. However, the direction of polarization can be altered through an applied electric field. When an external field is applied to a ferroelectric material it first responds dielectric until the electric field is strong enough to start to
switch all domains (following the virgin curve A in Figure 5). The polarization is now saturated (B). If the applied electric field is increased further, the material responds dielectric (B-C). If the electric field is reduced to zero, some of the domains switch back to their original states in order to lower the stored elastic and electrostatic energies. However, most of the switched domains will remain in the positive direction and the crystal will exhibit a macroscopic remanent polarization \( P_r \) in absence of an applied field. The extrapolation of the dielectric line segment after saturation (B-C) gives the spontaneous polarization at zero fields \( P_s \). This would be the remanent polarization without relaxation of the domains.

The remanent polarization \( P_r \) cannot be removed at ambient temperature until an electric field in the opposite direction is applied. At a certain negative electric field some of the domains switch in the other direction so that the sum of the total polarization cancels \( (P(E_c)=0) \). This field is called the coercive field \( E_c \). The coercive field is dependent on the quality of the ferroelectric crystal. Defects such as inclusions or vacant sites pin the domain walls. The pinning increases the coercive field of the ferroelectric hysteresis loop and decrease the amount of polarization in the ferroelectric. Non-switching domains locked by pinning cause the drop in remanent polarization.

![Figure 5: Characteristic non-linear polarization curve (Hysteresis) found in ferroelectric materials. The fundamental parameters connected to the hysteresis are also marked. \( E_c \) coercive field, \( P_r \) remanent polarization and \( P_s \) saturated polarization.](image)

### 2.2. Basic Concepts of FeRAM Operation

In a dielectric capacitor of a DRAM, positive and negative charges will be displaced from their original position upon the application of an electric field. This displacement or polarization will vanish when the electric field return back to zero (left side in Figure 6). In a ferroelectric material used in a FeRAM, on the other hand, there is a spontaneous polarization. This polarization or displacement is inherent to the crystal structure of the material and does not disappear in the absence of the electric field (right side in Figure 6). In addition, applying an appropriate field can reverse this polarization. This behavior results in a hysteresis
curve. The information stored in the two possible polarization states can be read by applying a voltage pulse. Depending on the stored information, the charge or current flow will be different for switching or non-switching of the polarization state (Figure 7). By using a sense amplifier and a reference value, the current flow for switching and non-switching will be differentiated. Due to a possible switching during read, the information of the capacitor can be destroyed (destructive read out - DRO) and has to be restored by another pulse.

**Figure 6:** Comparison of information storage for DRAM versus FeRAM.

Another type of ferroelectric memory but with non-destructive read out (NDRO) and only one transistor per cell without any other passive or active elements, has a ferroelectric layer embedded in a metal-insulator-semiconductor structure. For this memory the two directions of the remanent polarization of the FeRAM cell: remanent polarization for information storage (without external electrical field or voltage).
ferroelectric layer control the surface conductivity of a silicon substrate. This memory is called metal-ferroelectric-semiconductor field effect transistor (MFS-FET) [Shi98b] [Fuj97a] [Tok99] [Xio99].

To polarize the ferroelectric capacitor positive and negative voltages are necessary. There are two possibilities in FeRAM design to achieve this: the pulse concept and the mid-level (VDD/2) concept [Bra99] [Roe00]. In the pulse concept, both sides of the ferroelectric capacitors are switched and the full voltage swing is applied across the capacitor. However, the relatively big plate capacitance has also to be switched, and the pulse plate pulsing may be slow and may cause disturb pulses. In the mid-level (V_{DD/2}) concept, one electrode of the ferroelectric capacitor is kept at a constant voltage and only one electrode of the capacitor is switched. Therefore, only half the voltage swing is applied across the capacitor. Also, leakage current can cause loss of polarization since both electrodes have to be at the same potential (V_{DD/2}) when no voltage should be applied to the capacitor.

The simplest structure for a ferroelectric memory cell is just like in a DRAM - a one transistor and one capacitor (1T/1C) cell. However, there are problems with these 1T-1C cells. Fatigue (gradual decrease of remanent polarization after repeated cycling of the ferroelectric), imprint (development of an internal field causes a shift of the hysteresis loop) and retention (decrease of relaxed polarization) of the ferroelectric capacitor can cause a bit failure. A 2T-2C cell where each bit has its own reference is more stable against these issues. While the 2T-2C circuit is not suited for high density application because it uses up much more space, it has the advantage that the reference cell fatigues or deteriorates at the same rate as the addressed cell and has double the signal compared to 1T-1C cell.

2.3. The Strontium-Bismuth-Tantalate Compounds

Stoichiometric SBT is defined as SrBi$_2$Ta$_2$O$_9$. The variation in cation composition in non-stoichiometric SBT makes it possible for SBT compounds to adopt a number of different crystal structures. Non-stoichiometric SBT is either formed during the manufacturing or from a deliberate deviation in the concentration of the precursor. Stoichiometric deviations connected with manufacturing are supposed to depend on either the high volatility of Bi$_2$O$_3$ or Bi interaction with the Pt electrode [Fuj98]. After SBT has depleted in Bi, it is unable to form the highly complex bismuth layered perovskite that is the only known ferroelectric phase within the SBT system. In order to form the Bismuth-layered Perovskite the constituent materials must transform from the initial amorphous phase into a super lattice.

Primary Phases

As deposited SBT has an amorphous microstructure with a random distribution of cations with a maximal number of coordinating oxygen atoms. The amorphous microstructure is metastable and starts to crystallize at 500-550°C for 1:2:2 SBT [Rod97].
The first crystal structure that forms between 500-650°C in the SBT system is believed to be the simple Fluorite structure [Fuj98] [Osa98] [Lee99d]. The structure is named after the mineral Fluorite CaF$_2$, which is a common structure for binary compounds in which the cations support eight-fold anion coordination. However, the Fluorite structure in the SBT system has only one eight fold coordinated cation site within its lattice. Sr$^{2+}$ and Bi$^{3+}$ are able to form stable eight-fold oxygen coordination, whereas the smaller Ta$^{5+}$ would prefer an octahedral coordination. SBT compounds, therefore, tend to form a defective fluorite structure in which Sr, Bi, and Ta are surrounded by six (not 8) oxygen ions [Sco98]. Hence TaO$_6$ octahedra already exist in the fluorite phase. Therefore, it is believed that the transformation between amorphous SBT and the complex Bismuth-layered Perovskite goes through the fluorite structure [Har98a]. The defective oxygen coordination gives the SBT-Fluorite structure a metastable nature. This fact together with the random mixing of cations within the lattice are the fundamental properties that allow the fluorite phase to act as an intermediate phase during the crystallization of Bismuth-layered Perovskite [Rod97]. Even though most of the fluorite transforms at temperatures higher than 650°C, lateral deviations in the microstructure have been observed, with residual fluorite and secondary phases at grain boundaries [Lee99d] [Koi96].

![Figure 8: Ternary phase diagram showing stable phases in the SBT system [Gut96] [Bac01]. The reference point for stoichiometric Aurivillius SBT is SrBi$_2$Ta$_2$ or Ta=2/5, Bi=2/5 and Sr Sr=1/5. The dashed line goes through the stoichiometric SrBi$_2$Ta$_2$ point and corresponds to varying Bi content with Sr/Ta always being the same: SrBi$_x$Ta$_2$ with x=0→∞. The pyrochlore phases are found with less Bi (Bi<2/5) and the fluorite phases with excess Bi (Bi>2/5) [Rod96].](image)

The Pyrochlore structure is a derivative of the fluorite structure. The ideal Pyrochlore structure has an ordered arrangement of oxygen vacancies leading to a cubic unit cell composed of eight fluorite type cells [Rod97]. The formation of the Pyrochlore phase may be induced by non-stoichiometric SBT, type of precursor, solvent and the processing conditions [Zha99]. A fundamental difference between the fluorite and the Pyrochlore structure is that the latter has been prepared as a powder, whereas the former only has
been observed in layers [Rod96]. The ability to generate powder sample indicates that the Pyrochlore is not likely to be a metastable compound. The Fluorite phase changes to Bismuth-layered Perovskite or to the Bismuth deficit Pyrochlore phase after heat treatment above 700°C [Rod97] [Osa98]. If the SBT composition is sufficiently low in Bismuth content, it is very likely that the Pyrochlore phase will form. Due to the relative stability of the Pyrochlore phase and the low concentration of Bismuth within the lattice, it is unlikely that a transformation from Pyrochlore into the Bismuth-layered Perovskite will occur. A remedy for the Bismuth loss during the manufacturing is an additional surplus of Bismuth to the precursor. Change in bismuth contents with strontium and tantalate relation hold constant (Sr:Ta 1:2) is visualized by the black line in Figure 8.

Figure 9: (a) TEM picture of the Aurivillius phase with the Bismuth oxide-double layers marked with arrows. (b) Schematic structure of the Aurivillius phase indicating the ferroelectric active Perovskite unit A [Cho99].

The Bismuth-layered Perovskites

The Bismuth-layered Perovskites includes a broad family of compounds with the molar relation \((\text{Bi}_2\text{O}_2)^{2+} (\text{A}_{x-1}\text{B}_x\text{O}_{3x+1})^{2-}\) [Smo61] [Sub62] [Ara95] [Par99]. Where A can be mono-, di- or trivalent ions or a mixture of them (Ba, Sr, Pb), B can be \(\text{Ti}^{4+}, \text{Ta}^{5+}\) or \(\text{Nb}^{5+}\), and \(x\) can have values of 2,3,4 etc. This gives nine different molecular combinations. The B site cation is ferroelectrically active and has strong interaction only on the two dimensional sheet perpendicular to the c-axis. As a result the ferroelectricity of Bismuth layered Perovskites is highly anisotropic [Rav97]. The two-dimensionality in this group of
material is supposed to come from the weak Bi-O p-π bonding, compared to the stronger bonding in the Perovskite layer [Fuj98]. Spontaneous polarization in layered Perovskites can be ascribed both to the displacement of the B cations as well as tilting of the BO$_6$ octahedra [Shi99b].

The Aurivillius phase is a part of a Bismuth-layer-structure-family first described by Aurivillius in 1949 [Smo61] [Sub62] [Ara95] [Rod96]. These structures can be considered in terms of alternating layers of rocksalt (Bi$_2$O$_2^{2+}$) and Perovskite (SrTa$_2$O$_7^{2-}$) units. The Bismuth-Layered Perovskite SrBi$_2$Ta$_2$O$_9$ is best described by the orthorhombic space group, with lattice parameters c=25.09Å a=5.82 Å b=5.26 Å [Kle95]. Due to the small difference between a and b some authors suggest that the unit cell should be pseudo tetragonal. The TaO$_6$ octahedra in one Perovskite layer has an off-set in comparison with the TaO$_6$ octahedra in the neighboring Perovskite layer so that the c-axis of the unit cell includes two Perovskite layers following the ABAABA stack (Figure 9) [Cho99] [Auc98], where A designates a layer of TaO$_6$ octahedra and B a Bi$_2$O$_2$ layer. The strontium cations occupy a twelve fold coordinated sites in the space between the TaO$_6$ octahedra in the Perovskite sub lattice. Phase separation to Aurivillius phase and micro grain regions with fluorite or Pyrochlore begins with heat treatment above 700°C [Fuj98] [Rod97] [Osa98] [Koi96].

<table>
<thead>
<tr>
<th>SBT</th>
<th>Sr</th>
<th>Bi</th>
<th>Ta</th>
<th>O</th>
<th>Ti</th>
<th>Pt</th>
<th>TiO$_x$</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>density [g/cm$^3$]</td>
<td>6.842</td>
<td>2.6</td>
<td>9.8</td>
<td>16.6</td>
<td>4.5</td>
<td>21.45</td>
<td>4.05</td>
</tr>
<tr>
<td>2</td>
<td>molar mass [g/mol]</td>
<td>87.62</td>
<td>208.98</td>
<td>180.95</td>
<td>16.0</td>
<td>47.88</td>
<td>195.08</td>
<td>79.9</td>
</tr>
<tr>
<td>3</td>
<td>Possion's ratio $\nu$</td>
<td>0.361</td>
<td>0.39</td>
<td>0.42</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>bulk modulus $E/(1-\nu)$ [GPa]</td>
<td>108.4</td>
<td>276</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>expansion coefficient $\alpha$ [10E-6 K$^{-1}$] 20-100°C</td>
<td>8.9</td>
<td>9.0</td>
<td>2.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>expansion coefficient $\alpha$ [10E-6 K$^{-1}$] 20-1000°C</td>
<td>8-10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>s/h/(T2-T1)=<a href="%5Calpha-%5Calpha_Si">E/(1-\nu)</a> [MPa/K]</td>
<td>0.7</td>
<td>1.77</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>melting point [°C]</td>
<td>770</td>
<td>271.3</td>
<td>2996</td>
<td>1660</td>
<td>1772</td>
<td>1850</td>
<td>1410</td>
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<tr>
<td>9</td>
<td>boiling point [°C]</td>
<td>1375</td>
<td>1560</td>
<td>5425</td>
<td>3287</td>
<td>3827</td>
<td>2355</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>mass per unit area of SBT/Pt/Ti [µg/cm²]</td>
<td>121.217</td>
<td>9.670</td>
<td>52.8</td>
<td>41.7</td>
<td>17.047</td>
<td>4.507</td>
<td>210.90</td>
</tr>
<tr>
<td>11</td>
<td>thickness [nm]</td>
<td>177.17</td>
<td>37.2</td>
<td>53.9</td>
<td>25.1</td>
<td>10</td>
<td>98.3</td>
<td></td>
</tr>
</tbody>
</table>

Bismuth-layered Perovskites have large polarization along the a or b axis, but no polarization along the c-axis. Because SBT is a highly uniaxial ferroelectric (c/a>>1) it does not generally exhibit 90° domains. The domain structure consists mostly of ribbon-like rectangles of 180° domains [Sco98] [Ama95]. The extremely good fatigue resistance of the Bismuth-layered Perovskite is thought to depend on the net

Figure 10: Summary of physical and mechanical properties for all relevant elements of the Pt/SBT/Pt/Ti capacitor module. Values in the box are taken from www.goodfellow.com and values for SBT are obtained from XRF measurements. The thickness values in line 11 are calculated from line 10 and line 1: mass per unit area [µg/cm²] / density [g/cm³] = thickness [10$^8$ m].
electric charge of the rock salt layers \((\text{Bi}_2\text{O}_2)^{2+} (\text{A}_{x-1}\text{B}_x\text{O}_{3x+1})^{2-}\). Their position in the lattice is self-regulating to compensate for space charge \(V^0_{\text{O}} (2+)\) (oxygen vacancies) that are normally found in oxide films near the electrodes [Ara95]. Bismuth oxide is well known to minimize interlayer stress. It is also known that super lattice compounds have a unique ability to convert point defects into strain lattice planes that are less likely to pin domains and degrade switched charge [Auc98]. The \(180^\circ\) domain configuration also helps to avoid fatigue, as a \(90^\circ\) domain is more likely to be pinned than a \(180^\circ\) domain [Ama95]. All these features contribute to the extremely good fatigue resistance of SBT films. The Curie temperature for stoichiometric SBT is about \(300^\circ\)C whereas Sr deficiency and Bi excess can give Curie temperatures as high as \(400^\circ\)C [Shi99b].

In Figure 10 different physical and mechanical properties for all relevant elements of the Pt/SBT/Pt/Ti capacitor module are shown. The density of SBT of 6.8g/cm³ is comparable to the density of e.g. \(^{24}\)Cr (7.1g/cm³), \(^{40}\)Zr (6.5g/cm³), \(^{51}\)Sb (6.7g/cm³), \(^{58}\)Ce (6.7g/cm³) and \(^{30}\)Zn (7.1g/cm³).

### 2.4. Challenges in integration of ferroelectric thin films

Without considering the following list as complete, a few of the major issues in the development of high-density ferroelectric memories shall be addressed here.

#### Choice of ferroelectric material

Since low-density devices with both PZT [Phi96] [Ito00] and SBT [Sum95] [Fuj97b] material are already on the market, the functionality of the materials in integrated FeRAM circuits with the so-called offset technology (see Figure 11) is already proven. However, up to today, no products are commercially available with the stack technology (see Figure 12). This implies that fundamental integration issues for high density FeRAMs have to be solved first and it does not seem that these issues are correlated to a specific ferroelectric material. Comparing PZT and SBT, every material has its own advantages and disadvantages. PZT shows severe fatigue on platinum electrodes after \(10^6\) writing cycles [Kin96] in comparison with SBT that does not show severe fatigue before \(10^{10}\) cycles. PZT however, has the advantage of a much lower processing temperature and a higher remanent polarization \(2P_r \sim 50\mu\text{C/cm}^2 @ 5V\) for PZT versus \(2P_r \sim 20\mu\text{C/cm}^2 @ 5V\) for SBT). These properties have impact on the development and the reliability concerns of high density FeRAMs. Although there might be later a few differences in integration between PZT and SBT - just like in the DRAM world between stack and trench integration - but once the basic issues mentioned below have been solved and the ideal process routes are identified, a high density FeRAM should be realizable regardless of its ferroelectric material.
**Oxygen barrier stack**

A typical FeRAM stacked capacitor cell structure is shown in Figure 12. The capacitor module is connected with the transistor module via a plug module. Between the plug and the capacitor module, a barrier is needed to avoid oxidation of the plug material as well as inter-diffusion of species between the capacitor module and the transistor area. Due to annealing temperatures of 550-700°C necessary for the formation of the ferroelectric phase, polysilicon plug material in combination with high temperature barriers based on new materials like Ir/IrO$_2$ is usually used [Nag01] [Mik01] [Sco95] [Gna94] [Pin01] [Jun99]. Conventional barrier materials like TiN, TaN or alloys of TiN or TaN with Si or Al can only be used in a temperature range of 450-600°C [Moi99].

**Bottom electrode system**

To prevent oxidation of the metal electrodes at the high processing temperatures in oxygen needed to crystallize the ferroelectric, a noble metal like Pt or Ir has to be used. For SBT Pt is mainly used whereas for PZT IrO$_x$ or (Sr)RuO$_x$ [Kin96] have to be used to compensate for the oxygen vacancies which are considered as the root cause for fatigue of PZT on Pt electrodes. Due to the chemical inertness of the noble metals, no interaction or interdiffusion with the most important interlayer dielectric SiO$_2$ is seen. This results in poor adhesion. Therefore, processing of ferroelectric material is frequently accompanied by peeling. For the offset cell structure (see Figure 11) or for test structures, Ti is commonly used as an adhesion material between SiO$_2$ and Pt. However, due to the high reactivity of Ti, an interaction of the SBT-Pt-Ti system is seen. The effect of Pt/Ti bottom electrodes on microstructural and electrical properties of SBT thin films will be discussed in chapter 4.

**Deposition of ferroelectric thin films**

The composition and orientation of the ferroelectric films greatly affects the ferroelectric properties of the capacitor. It is therefore important to control these features in order to obtain excellent ferroelectric properties. Size and shape of the ferroelectric grains can be regulated by deposition parameters. In chapter 5, SBT layer processing deposited by Metal Organic Decomposition (MOD) (see chapter 3.1) will be evaluated. Physical and electrical properties of SBT thin films versus film thickness, anneal sequence, anneal temperature and anneal ambience will be studied.

For high density FeRAM applications, PZT or SBT deposition will eventually require methods like metal-organic chemical vapor deposition (MOCVD) in order to achieve the required step coverage of $\geq50\%$ instead of other deposition techniques like MOD or sputtering deposition. MOCVD SBT processes are described in [Hin98] [Iso97] [Bac01] and MOCVD processes for PZT in [Sak00]. For future devices and to demonstrate lateral and vertical scalability, the switching behavior of integrated ferroelectric thin films
down to e.g. 0.1µm and 50nm respectively have to be shown [Moe02] although preliminary AFM studies on ferroelectric thin films look promising [Pig00] [Ale99] [Gan99] [Har00c] [Gru97] [Gru99].

**Patterning and etching of noble metals and ferroelectric thin films**

One of the main process objectives in the integration of ferroelectric capacitors into memory devices is the development of patterning processes for ferroelectric films and electrodes. The use of ceramic materials and noble metals introduce new issues for patterning. Due to their chemical inertness, etch processes for e.g. Ir, IrOx, Pt, PZT, SBT, ... are extremely challenging. Also, advanced patterning methods are necessary to achieve vertical sidewalls. The effect of SBT capacitor formation or patterning processes together with the influence of the recovery anneal on physical and electrical properties will be discussed in chapter 6.

**Hydrogen sensitivity and barrier layers**

Many integration processes in semiconductor industry can degrade the ferroelectric performance of ferroelectric capacitors. This is mostly due to hydrogen impregnation during deposition of interlayer dielectric, tungsten-plug and passivation processes. In addition etch damage and mechanical stress imposed by various layers on these capacitors can alter the ferroelectric properties. Since oxide ferroelectric materials are very easily reduced by reductive ambient like hydrogen, processes for the integration of encapsulation barrier layers (EBL) to protect the capacitor module against hydrogen deterioration originating from backend of line (BEOL) processing have to be found. Degradation mechanisms of SBT thin film capacitors in a hydrogen ambience (forming gas) will be studied in chapter 7.

**Other issues**

Other major challenges of the modular technology concept with inserting the ferro capacitor module while leaving the other processes unchanged, are: impact of high temperature anneals on the characteristics of transistors, influence of e.g. “lead on chip” assembly like bonding (e.g. 300°C, 1s) and molding (e.g. 4h, 175°C, 110bar for 6-10s), impact of integration on reliability like fatigue, imprint, and so on (especially at elevated temperatures), integration of 3D capacitor features for ultra high density devices to increase the signal margin, and huge aspect ratios of equal or more than 3.5 for contacts to gate and diffusion.

**The market place**

FeRAMs need to be competitive at a $/bit level in a highly cost effective environment in order to replace existing technologies. This means that the technology has to meet the potential of a 30% p.a. long term
price degression and a 25-30% p.a. shrinkage demand as typically seen in DRAM business. Therefore, FeRAMs can only be competitive if a smaller cell size and/or improved performance is offered. In order to keep FeRAM technology development and processing costs low, conventional frontend and backend processes should be used in combination with only one new module, the capacitor module. The 1T/1C cell or smaller like chain FeRAM (see next chapter) is a must. Depending on the base process used which can be either DRAM or logic, the FeRAM can have either a small DRAM-like cell size (≤13F^2) – with F being the minimum feature size on the chip - or the performance of a logic process together with a relatively large cell size (≈ 30F^2). However, even in the latter case, the cell size is still superior to a SRAM cell which is typically >60F^2.

**Contamination**

Of major concern for the manufacturer of semiconductor devices is the contamination aspect of the new materials. The use of high-k dielectric materials like BST or ferroelectric materials like PZT or SBT will introduce for instance alkali earth metals like Ba and Sr in standard semiconductor production lines. Platinum is relatively well known because power devices are intentionally doped with this element in order to control the switching speed but the use of platinum electrodes are not known to the semiconductor memory industry. It is well known that metal contaminations increases the leakage current which is a major issue for all DRAM manufacturer due to refresh failure. For Sr, Bi and Ba no drastic decrease in lifetime up to a contamination levels of 10^{14}at/cm^2 were found [Bou00a] [Bou00b]. Therefore, these materials are not considered a risk on minority carrier lifetime and diode leakage in future FeRAMs or high-k DRAMs. However, when Pt is diffusing into metal-oxide-semiconductor (MOS) structures, it is observed, that positive mobile Pt ions are introduced into the SiO\textsubscript{2} films and the density of states at the Si-SiO\textsubscript{2} interface is increased [Den95]. However, no gate oxide integrity (GOI) degradation was seen [Mer99]. Wet chemical cleaning experiments have only an effect on the wafer surface. If Pt or any other elements have diffused into the Si bulk e.g. by temperature treatment, it is no longer accessible to decontamination. Unfortunately, from all the new elements, Pt contamination on Si wafers cannot be removed completely by any wet cleaning [Pam00]. The noble Pt is hardly oxidized but easily re-deposited on a reactive Si surface.

### 2.5. Advantages and disadvantages of the main integration concepts

The most common integration concepts used in today’s low density FeRAMs are based on the so-called “offset cell” or “strap cell”. The ferroelectric capacitor is placed over the LOCOS isolation and connected via the top electrode and two contact holes to the access transistor (see figure 11). This structure is used for instance by Ramtron, Matsushita [Fuj97b], Motorola [Moa94], Hitachi, Fujitsu [Ito00], Toshiba,
Rohm, Hyundai and Infineon [Deh99]. The advantage of the offset integration concept is that no oxygen barrier underneath the bottom electrode is needed since all high temperature anneals in oxygen are performed before opening and filling the contact hole with W or poly-Si which could be oxidized. However, the major disadvantage of the lateral concept is the large cell size, which is not suited for high-density integration.

For realization of high-density memories the “stack cell” is a must. In this case the ferroelectric capacitor sits on top of the poly-Si or W-plug connected to the transistor (figure 12, figure 13 and figure 14). Now a stable oxygen barrier on top of the plug is needed in order to prevent the oxidation of the plug. The tradeoffs of the very small stack cell are the oxygen barrier and the etching process with its added complexity. The ferroelectric capacitor can either be etched in a multiple mask layer process [Jun99] [Nak98] [Lee99c] (figure 12a) or by an “one step capacitor etch” [Kac98] [Moi99] [Sam00] (figure 12b). The “one
step capacitor etch” allows a smaller cell size than the multiple layer mask process. However, for the “one step capacitor etch” concept (figure 12b) an advanced hot cathode etching process with a hard mask has to be used whereas for the other standard etching processes with standard photoresist can be used (figure 12a). Both concepts shown in figure 12 are based on a planar capacitor. In figure 13a, a 3D capacitor is shown. The main difference between the concepts of figure 12 and figure 13a is that for the 3D integration the bottom electrode stack has to be patterned prior to deposition of the ferroelectric material. This means for the 3D integration that the high temperature crystallization anneal in oxygen is performed with only minimal overlap of the oxygen barrier over the plug causing oxidation of the plug from the side. For the 2D integration shown in figure 12 this problem does not exist since the crystallization anneal is done with the bottom electrode stack left unpatterned. The capacitor is etched after the crystallization anneal. In the future ways have to be found to realize the 3D capacitor to increase the charge for ultra high memory densities.

Figure 13: Vertical high density FeRAM stack cells with a) 3D capacitors and b) capacitor-on-metal/via-stacked-plug (CMVP) above metal 2 as shown by NEC [Ama98].

NEC has developed a memory cell with a capacitor on a metal via stacked plug called CMVP concept (figure 13b) [Ama98] [Ama00]. The ferroelectric capacitor is formed above metal 2 at the end of standard CMOS process and is connected to the transistor via aluminum metal and stacked W plug. Therefore, no modification to the CMOS logic device is necessary and only a passivation after the ferro module is needed. The production line can be shared with other logic devices making this concept very attractive for embedded FeRAM applications. However, due to the Al metallization before processing the ferro module, no high temperature process above 450°C is allowed. An ultra low temperature deposition and crystallization process for the ferroelectric layer has to be developed.
The Chain FeRAM concept (CFeRAM) has been introduced by Toshiba in 1997 [Tak97] [Tak98] [Tak99] [Bra99]. Toshiba will use this concept together with thin SrRuO$_3$ films within both platinum bottom and top electrodes to improve fatigue characteristics [Mor00] for future FeRAM devices. In CFeRAM’s a memory cell consists of a parallel connection of one transistor and one ferroelectric capacitor (Figure 14). N cells in series are combined to a memory block (i.e. 8 cells). One end of the block is connected to a cell plate line (PL) (left side in Figure 14) and the other end is connected to a bit line (BL) via a block selecting transistor (right side in Figure 14). The effective cell size per bit for the CFeRAM concept is only $4F^2+X$ (some $X$ comes from the additional block selecting transistor), compared to the minimum cell size of $8F^2$ for the standard stack cell (e.g. figure 12). During standby, all cell transistors are turned on, shorting all ferroelectric capacitors and shielding the capacitors from disturb pulses. In the active cycle, the word line of the selected memory cell is pulled down, and the word line of the block-selecting transistor is pulled up. Now a switching or non-switching charge will flow trough the selected memory capacitor to the bit line and then to a sense amplifier. Again, the read operation is destructive (DRO) and a write back is necessary. The access time to the bit is increased due to the series resistance in the chain.

![Figure 14: Concept of the chain FeRAM (CFeRAM) with a 4F² cell as introduced by Toshiba.](image-url)
3. Experimental Techniques

3.1. Metal Organic Decomposition (MOD) and capacitor formation

In this chapter all processes used to produce standard ferroelectric SBT capacitors on silicon wafers are described. All of the following process steps were used for the electrical characterization of the capacitors. Only a few of the process steps may have been used for studies of other physical properties. As usual, all layer sequences are given beginning with the top layer.

![Top view SEM pictures of the process steps](image)

Figure 15: Top view SEM pictures of (a) Pt(200nm)/Ti(20nm)/SiO2/Si after dep., (b) after annealing at 650°C in O2, (c) after SBT coating plus RTP, (d) plus crystallization anneal at 800°C, (e) after Pt top electrode dep and (f) after post anneal at 800°C. Note the grain growth of platinum after the 650°C and 800°C anneal in b and f.

First, a wet oxide of 625nm was grown on Si-substrates. Then, the bottom electrode was formed with thicknesses of 10nm Ti and 100nm Pt sputtered in-situ using a DC magnetron sputtering system (see
Patterning of the bottom electrode was performed in a Magnetically Enhanced Reactive Ion Etching (MERIE) reactor of a multichamber cluster tool using standard photo-resist mask (see RIE). The electrodes were then pre-annealed at 650°C in dry oxygen. SBT was deposited using a spin-on process with an MOD solution (see MOD). To avoid contamination by diffusion of Pt, Sr, Bi and Ta atoms, a backside etch clean was performed after the hot plate bake before high temperature RTP annealing. The RTP process was at 725°C (650°C) for 30s in O₂ (the temperature value in the brackets refer to a low temperature process). It was found, that the time between spin coating and the RTP process step should not exceed a few hours. E.g. waiting for one day resulted in low polarization values and high leakage currents. After two SBT coatings, backside etches and RTP process steps, the samples underwent a crystallization anneal at 800°C (700°C) in O₂. The resulting final film thickness was 180nm. Afterwards, a Pt top electrode of 200nm thickness was sputtered. After patterning of top Platinum and SBT bilayer in the MERIE reactor and removing the resist mask in a downstream asher, a final anneal at 800°C (700°C) in O₂ was performed to recover the damage caused by the etching process. All anneals were performed in a quartz tube furnace in an O₂-atmosphere with a flow of 5l/min. Forming Gas Anneals (FGA) in chapter 7 were done in a quartz tube furnace in a (N₂, 5% H₂)-atmosphere at 430°C for 30min with a flow of 5l/min.

In Figure 15 SEM pictures of the surfaces after each layer deposition and each thermal treatment can be seen. The Platinum grain size of the top electrode before annealing is less than 100nm whereas the grain size after annealing is about 400nm. The corresponding SEM cross-section are shown in Figure 19 on page 40.

**Metal-Organic Decomposition (MOD) or Chemical Solution Deposition (CSD)**

The composition and orientation of the SBT films greatly affects the ferroelectric properties of the capacitor. It is therefore important to control these features in order to obtain excellent ferroelectric properties. Size and shape of the SBT grains can be regulated by deposition parameters [Cho99].

Metal-Organic Decomposition (MOD) is a non-vacuum, liquid based, spin-on method for depositing thin films using metal-organic precursors [Man89]. Common for sol-gel and MOD technique is the decomposition of metal alkoxides to produce oxides. However, the sol-gel technique strictly refers to solutions in alcohol, which undergo gel formation, whereas MOD does not [Sco00]. Therefore, the new term Chemical Solution Deposition (CSD) has recently been used, to summarize all wet-chemistry deposition techniques like MOD, sol-gel, MOCVD in contrast to the physical deposition such as sputtering or MBE. Metal-organics are described as coordinate covalent compounds with a metal atom bonded to an organic liquid via a bridging oxygen, sulfur, phosphorus, or nitrogen atom. The metal-
organic SBT precursor\textsuperscript{1} [Sco96], dissolved in solution\textsuperscript{2}, was dispensed onto the substrate much like a photoresist. For coating the substrate was spun at 1800 revolutions per minute for 30s to remove the excess fluid, to drive off the solvent, and to uniformly coat the substrate surface with the organic film. The film thickness after coating is a few microns. Theoretical descriptions of the spin-on process versus spin-speed, viscosity, solvent evaporation and so on can be found in [Bor89] [Fla84] [Gu96] [Hal98]. The soft metal-organic film was then pyrolyzed in air, oxygen [Uch00] or nitrogen [Fai98] to convert the metal-organic precursors to their constituent elements, oxides, or other compounds. In our case two hot plate baking cycles were used: 1\textsuperscript{st} 160°C 1min., 2\textsuperscript{nd} 260°C 4min. During this thermal decomposition, there is a substantial vertical shrinkage of the percursor film thickness. The degree of shrinkage depends on the number and length of the hydrocarbon chains attached to the metal atoms. Therefore, large and many cracks were often seen in films after the pyrolysis of SBT precursors films thicker than 120nm. Consequently, the SBT layer was deposited with 2 layers each having a thickness of 90nm to achieve the standard target thickness of 180nm after crystallization anneals.

The composition of the SBT before coating was Sr=0.974, Bi=2.155, Ta=2.0 and after coating and crystallization annealing Sr=0.965, Bi=2.118, Ta=2.0 as measured by ICP. The lower Bi content of the films compared to the original solution is due to Bi loss during annealing.

The rate of volatiliy of the precursors or solvent, the thickness of the unpyrolyzed film, the rate of pyrolysis, and the annealing temperature influence the formation of quality films by MOD. The MOD process allows the deposition of very homogeneous films with a thickness uniformity $\sigma$ of $<$5\% on a planar wafer (with $\sigma$ being the standard deviation). The chemical constituents or dopants may be adjusted by varying the concentration of the precursor materials added to the solution. All this adds up to a simple, inexpensive means of film deposition that is compatible with VLSI technology.

\textbf{Physical Vapor Deposition (PVD)}

Physical Vapor Deposition process was originally developed to deposit materials with a very high melting point (so called refractive materials). Sputtering involves the removal of material from a solid cathode called target. This is accomplished with Ar gas plasma. The ions are accelerated and knock some of the cathode material loose from the surface. The material is transferred into a physical vapor that deposits on the substrate. The film thickness of the deposited material can be controlled by the sputter time and power. In addition to refractive materials, sputtering is very useful for the deposition of alloys and compound

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\textsuperscript{1} Sr[OCOC$_7$H$_{15}$]: Strontium 2-ethyl hexanoate (8\% by volume), Ta[OCOC$_7$H$_{15}$]: tantalum 2-ethyl hexanoate (25\% by volume), Bi[OCOC$_7$H$_{15}$]: bismuth 2ethyl hexanoate (37\% by volume), C$_7$H$_{15}$ n-octane (30\% by volume), C$_8$H$_{18}$COOH 2ethyl hexanoic acid (trace amount), butanol (trace amount) [Ara96] [Koj96]. This solution is a light brown liquid.
materials as the resulting film structure can be tailored closely to match the composition of the starting target material.

All platinum films of different thickness were deposited from a source with 99.99% purity by a Endura HP DC magnetron sputtering system from Applied Materials Corp. The tool was also equipped with a titanium chamber attached to the mainframe. For wafer handling and process control preclean, cooldown, degas/orienter and transfer chambers were part of the sputter system. All chambers have cryo-pumped vacuum systems. The base pressure was <4·10⁻⁸ mbar. The depositions were made at different temperatures ranging from RT to 550°C. Typical PVD conditions for Pt were 4.8·10⁻³ mbar in Ar, 500W, deposition rate 1.52nm/s at 500°C, and for Ti 1.67·10⁻³ mbar in Ar, 6000W, deposition rate 1.43nm/s at 200°C.

**Heat processes (RTP and furnace)**

For rapid thermal processing, a SHS2800 RTP tool from AST/Steag Corp. with lamp heating is used. The wafers are placed individually in a quartz chamber and sit during annealing on quartz pins (single wafer tool). The gas is flowing horizontally around the wafer with a flow of 5l/min. The RTP process is used at atmospheric pressure for all anneals. Wafer temperature is monitored by a pyrometer from the backside of the wafer. Therefore, it is very important to calibrate the RTP for each desired wafer backside in use. Two main gases were used: oxygen (O₂) and nitrogen (N₂).

The annealing process can be differentiated in three phases: ramping or heating, annealing and cooling. Before heating the RTP is flooded for 30s with the desired gas. Then, the lamps are switched on and preheat is set at 400°C to allow the lamps to stabilize. Finally, the temperature is raised to the desired temperature. The standard ramp rate is 25°C/s. In the following step the wafers are annealed for the desired time. Cooling is usually done in the same gas as during annealing. At the end the chamber is purged with N₂.

For all crystallization anneals a PEO 603 furnace tool from ATV corp. with fast-ramping lamp heating is used. The furnace can be used at atmospheric pressure or with low pressure. The wafers are placed vertically in a quartz boat. The gas is flowing from the front to the back. Three main gases are supplied: oxygen (O₂), nitrogen (N₂), and forming gas (5% H₂, 95% N₂). The process gases were set manually to 5l/min.

Before heating the furnace is flooded for 10 minutes with the desired gas. Then, to avoid overshooting the chamber is heated to the desired temperature x°C minus 70°C, to x°C-30°C, to x°C-10°C and finally to x°C with a ramp rate of 1°C/s, 0.33°C/s, 0.17°C/s and 0.08°C respectively. After annealing at x°C for the

---

² n-butyl acetate to obtain SBT solution with 0.12M (not present in the original solution but was added just before spin-on deposition)
desired time, the gas is switched to nitrogen for the last 5 minutes before cooling. Standard cooling is done in a nitrogen atmosphere to avoid CMOS transistor damage. A fan inside the furnace does the cooling.

**Plasma dry etch (RIE)**

For anisotropic patterning of the bottom Pt/Ti and top electrode Pt/SBT stack a P5000 MxP R2 metal etch chamber from Applied Material Corp. was used. The film thickness of the photoresist was 1.1µm for the 100nm Pt bottom electrode and 1.5µm for the 200nm Pt top electrode. The bottom electrode was etched using chlorine (13.3×10⁻³ mbar, 750W, 80Gauss, 50sccm Cl₂) in an etch process with fixed time (72s for 100nm and 122s for 200nm bottom electrode). The top electrode and SBT stack was patterned with Ar (13.3×10⁻³ mbar, 750W, 80Gauss, 50sccm Ar) since etching of the Pt/SBT stack using chlorine gives high mask erosion of the photoresist, huge taper and poor electrical results. The Ar recipe for Pt/SBT etch was ended by an automatic endpoint system using insitu optical emission spectroscopy for detecting the clearing of SBT and the starting of Pt bottom electrode etch. The photoresist was removed in a strip chamber attached to the same mainframe as the etch chamber without venting. A typical “ash” recipe was: 1000W, O₂:N₂ 3000sccm:300sccm, 2.5-15min. For cleaning of organic residues a wet chemical process followed. For cleaning of the bottom electrode a EKC265 clean (commercial product from EKC Corp.) at 65°C for 15min is done. For the top electrode/SBT stack a RCA-1 clean (NH₄OH:H₂O₂ 1:9) at 55°C for 3.5min. is performed.

It is well known that strong photo mask erosion is obtained from chlorine plasmas during RIE [Fra94] [Man88]. This is supposed to depend on the fact that chlorine plasma attacks the photoresist more aggressively than argon due to its chemical reactivity. Additionally, intermediate redepositions of Pt etch products onto the mask sidewall lead to a low overall sidewall taper in the bottom electrode. On the other hand, argon etching of the top electrode is a purely physical etch process. Due to vertical impact of argon ions, no tapering is observed for Pt/SBT etching. High mask selectivity is thought to be caused by passivation from redeposition of SBT and platinum slowing down the mask erosion and thus preventing strong tapering. Therefore, with argon plasma sidewall angles of above 80° can be achieved whereas with chlorine plasmas normally sidewall angles of only 50° are obtained due to tapering. The main problem with argon etching is that mask sidewall redepositions remain after the removal of the photoresist. A post etch cleaning method is thus needed to remove the redepositions.

3.2. Characterization and measurement techniques

**Electrical Characterization**

Two different techniques are usually used to measure the remanent polarization of the ferroelectric capacitors: Virtual Ground and Sawyer Tower. The Sawyer Tower measuring technique is an established
method for the characterization of non-linear devices [Rad97]. The test configuration is composed of an external power source that applies a voltage over the ferroelectric capacitor and a reference capacitor (sense capacitor) connected in series as shown in Figure 16a. The Sawyer Tower measurement technique is based on the fact that two capacitors in series store the same charge \( Q = C_{\text{ferro}} V_{\text{ferro}} = C_{\text{ref}} V_{\text{ref}} \). \( V_{\text{ferro}} \) is the voltage over the Ferroelectric capacitor and \( V_{\text{ref}} \) and \( C_{\text{ref}} \) the voltage and capacitance of the sense capacitor respectively. If the voltages over the two capacitors are known as well as the capacitance of the sense capacitor, the polarization of the ferroelectric capacitor can be calculated

\[
P(E) = (\varepsilon_r - 1) \varepsilon_0 E = \frac{C_{\text{ferro}}}{\varepsilon_0 A} - 1 \varepsilon_0 E = \frac{C_{\text{ref}} V_{\text{ref}}}{\varepsilon_0 A V_{\text{ferro}}} - 1 \varepsilon_0 E
\]

[eq. 9]

In the Sawyer tower setup the depolarization current that flows through the ferroelectric capacitor is stored in the sense capacitor. When the applied voltage source returns to zero volt the stored charge in the sense capacitor generates a voltage that is applied in the opposite direction to the last drive voltage used. This is known as back voltage. The back voltage may be minimized by the proper selection of the sense capacitor value. A rule of thumb is the capacitance of the sense capacitor should be 10 times larger than that of the ferroelectric capacitor. For the hysteresis measurement using the Saywer Tower technique, a HP54815A Infinium oscilloscope and a Wavetec SD395 function generator were used. The operation of the instruments and the collection of the data were managed with the Symetrix Othello software application.

![Figure 16](image_url)

Figure 16: (a) The experimental setup of the Sawyer Tower test rig. \( V_{\text{ap}} \) is the applied voltage over the test rig. (b) The experimental setup of the virtual ground test rig.

The existence of a back voltage tends to tilt the measured hysteresis curves in comparison with those measured with the Virtual ground test rig, which takes account of both polarization current and voltage
over the test structure. In the Virtual Ground measuring system the sense capacitor is replaced with the measurement configuration shown in Figure 16b (Radiant RT6000S). The integrator circuit collects all current that flows through the ferroelectric capacitor as a result of the applied voltage and the polarization of the ferroelectric capacitor can be calculated

\[
P(E) = (\varepsilon_r - 1)\varepsilon_0 E = \left(\frac{C_{\text{ferro}} d}{\varepsilon_0 A} - 1\right)\varepsilon_0 E = \left(\frac{Q d}{\varepsilon_0 A V_{\text{ferro}}} - 1\right)\varepsilon_0 E = \left(\frac{\int I dt}{\varepsilon_0 A V_{\text{ferro}}} - 1\right)\varepsilon_0 E
\]  

[eq. 10]

The current consists of the polarization current and the leakage current. Normally the polarization current is much larger than the leakage current. In very leaky samples, however, this is not valid. In this case very bulky hysteresis curves are obtained. The influence from the leakage current on the remanant polarization can be avoided by a higher test frequency, which allows the depolarization current to pass, but not the leakage current. The Sawyer-Tower test setup uses a much higher test frequency (e.g. 10kHz) than the virtual ground test setup (e.g. 100Hz) due to oscillator restrictions. Therefore, the Sawyer-Tower test setup is insensitive to leakage currents. A leakage current measurement is done in connection with the virtual ground measurement to secure the validity of the measured polarization. For measurements of hysteresis loops a maximum amplitude of ±5V was used. From these loops the values for \(2P_r\) and \(2E_c\) are determined, with \(2P_r\) being the total remanent polarization and \(2E_c\) being the total width of the hysteresis loop.

For measuring the leakage current, voltages ranging from 0-10V in steps of 0.5-1V were applied to the sample with a hold time of 1s. A Keithley 230 programmable voltage source was used. The current was then measured with an Keithley 617 electrometer connected in series with the ferroelectric capacitor. The maximum current was limited at 2mA.

**Film Thickness Measurements**

Ellipsometry uses the reflection of linearly polarized light to measure the film thickness of thin films [Tom93]. Of primary interest is the phase shift of linearly polarized light upon reflection on a thin film. The phase shift is due to the difference in reflection coefficient for the field components parallel and normal to the plane of incidence. An ellipsometer measures the phase difference between the parallel and perpendicular component before and after reflection, and the intensity ratio between the perpendicular and parallel component after reflection. These two parameters can then be used to calculate thickness and index of refraction of the thin film with a proper model (e.g Cauchy model). The model can also handle multi-layer systems or multi-component layers. Porous films with many voids have to be considered as a two component. The models used for the calculation of thin films are based on planar layers of reflection. If the surface is rough or if the film is very porous, an accurate fit of the film thickness is not possible.
Therefore, only fitting results with a small error bar are usable. The advantage with ellipsometry is the possibility to measure both the index of refraction and the film thickness without anything else than a mathematic model of the surface reflection. Due to the relatively large surface needed for this method (5x15mm), ellipsometry is used only for non-patterned samples. The tool used was from SOPRA Corp. model ES4G with a wavelength from 250-930nm.

**Optical Reflectometry** is based on the interference between reflected light beams from the film and substrate surfaces [Tom93]. If the optical distance of propagation equals an integer multiple of the wavelength of the incident beam constructive interference occurs which results in a maximum of the reflected light intensity. A non-integer multiple of the wavelength gives destructive interference. A change of the wavelength will cause an oscillation of the reflected light intensity. If the dispersion relation of the wave length $n(\lambda)$ is known for the film material, the film thickness can be calculated with the help of Fourier transforms. In order to use the reflectometer the dispersion relation $n(\lambda)$ of the thin film has to be known. The dispersion relation is depending on the morphology and composition of the surface. Therefore the reflectometer has to be calibrated for each film using the desired substrate. The advantage with the reflectometer is the ability to measure the film thickness on patterned samples, as only a few $\mu$m$^2$ are needed for the measurement. Therefore all patterned samples where measured with the reflectometer. The tool used was from LEICA Corp. with a wavelength from 400-800nm.

**X-Ray Reflection** is like the optical reflectometry based on the measurement of the intensity of the reflected “light”. However, both dielectric and metallic materials can be measured. X-rays under grazing angles are used for different angles [Asp01] [Sch98]. Since the momentum transfer takes place in the scattering plane with components both perpendicular and parallel to the surface, the angle scans provide insight into lateral and vertical sample characteristics to determine film thickness, density, surface roughness, interface roughness, reaction zones and interdiffusion.

**Sheet Resistance Measurements**

Sheet resistance measurements were performed after sputtering and heat treatment of thin metallic films in order to determine crystallization, oxidation or interdiffusion. The sheet resistance $R_s$ is defined as the resistance per unit area of a film with a constant thickness $t$. $R_s$ is determined only by the thickness $t$ [cm] of the film and its resistivity $\rho$ [Ωcm], and is given by

$$R_s = \frac{\rho}{t} \quad [eq. 11]$$

in units of ohms. However, values for sheet resistance are usually given in units of ohms per square [Ω/sq.]. The most common method for measuring the resistivity $\rho$ of a film is the four-point probe method [Mur93]. In this method a constant current is passed between two outer probes, and the voltage drop
across the middle probes is measured. By properly selecting the probes, probe separations, and current, the voltmeter reading can directly give the sheet resistance $R_s$. The tool used was from Prometrix Corp.

**Residual Stress Measurements**

Residual stress measurements of blanket films were performed at RT after deposition and after annealing. The stress values $\sigma_f$ of the film are derived from the evolution of the wafer warpage. Assuming that the thickness of the film $t$ is much smaller than the thickness of the substrate $D$, the following equation is obtained to express the thin film stress \[\text{[eq. 12]}\]

$$\sigma_f = \frac{E_s \cdot D^2}{6(1-\nu_s) \cdot t} \frac{(R_1 - R_2)}{R_1 \cdot R_2}$$

where $E_s$ is Young’s modulus, $\nu_s$ Poisson’s ratio of the substrate and $R_1$ and $R_2$ are the radii of curvature before and after the deposition of the film respectively. The wafer warpage is obtained from a metrology tool from ADE corp. which is based on a technology employing two opposing capacitive probes to measure the distances from the probes to the front and the backside of a wafer. By stepping the wafer through these capacitive probes the curvature or radius of the wafer can be determined \[\text{[Zha95]}\] \[\text{[Sch98]}\].

**Stress versus Temperature Measurements**

The thin film stresses were analyzed by measuring the wafer warpage before and after film deposition using a Tencor FLX 2900 stress analyzer. In addition, this instrument is capable to measure the warpage of the wafer during a thermal cycle of the wafer up to 900°C. This system together with some background about thin film stresses is described in detail in \[\text{[Spi95]}\] \[\text{[Bru98]}\]. The heating rate for the wafers was 11K/min and the soak time at maximum temperature was 10min. The cooling rates were 11K/min between 800°C and 300°C, and 5K/min. between 300°C and 100°C.

**X-Ray Diffraction (XRD)**

X-Ray diffraction is a non-destructive test method for the characterization of crystalline phases. From the XRD spectra structural properties of the crystalline morphology can be determined such as degree of crystallization and orientation of crystal planes. XRD is based on the reflection of monochromatic X-rays on atoms. If the atoms are randomly distributed in the material the X-ray photons will be scattered in all directions. If on the other hand a long-range order in the solid exists, the reflected photons will not be randomly scattered but in some preferred directions. If the distance between two planes of reflection equals a multiple of the wavelength, constructive interferences occur defined by Bragg’s law of reflection \[\text{[eq. 13]}\]

$$n \cdot \lambda = 2d \cdot \sin \theta$$
where \( n \) is an integer multiple, \( \lambda \) is the wavelength, \( \theta \) the angle of incidence and \( d \) the distance between reflecting planes. The constructive interference is thus dependent on the angle of incidence and will show diffraction peaks when the right side of [eq. 13] equals the left. The intensity of these peaks depends on the amount of planes in the sample that are oriented with an inter-plane distance of \( d \). Through variation of the angle \( \theta \) different \( d \) will give its contribution to the constructive interference. In this way the orientation and lattice constant from a crystalline sample can be determined. From the width of the diffraction peaks further information about substitution of lattice atoms, stack faults, point defects and grain size can be determined.

![Figure 17: The XPS and Auger effect [Wal88].](image1)

![Figure 18: Setup of a commercial available pull tester [Bic98].](image2)

In order to investigate phase transformations that take place at higher temperature HT-XRD is used. HT-XRD is based on a normal XRD in which the sample is heated on a heat band to the temperature of choice. HT-XRD allows in-situ characterization of the structural change in the material. Either the sample is rapidly heated to the temperature of investigation and held at constant temperature or a temperature scan is performed.

**Auger Electron Spectroscopy (AES) and X-Ray Photoelectron Spectroscopy (XPS)**

Auger electron spectroscopy (AES) and X-Ray Photoelectron Spectroscopy (XPS) are well-established techniques to reveal the elemental composition of the outermost atomic layers of a sample (see e.g.
The two techniques are largely complementary. XPS is rather more sensitive and gives more information about the chemistry, while AES is faster and has a higher spatial resolution. AES is based on the Auger effect, which can be defined as a de-excitation of an ionized atom by a non-radiative process [Wal88]. A primary electron produces the excitation of an inner shell electron. An electron from one of the outer shells fills the vacancy in the inner shell. The difference in potential energies between the two states can either be released as characteristic X-ray photon (XPS), or be transferred to an Auger electron which is ejected from the atom with a characteristic energy (see Figure 17).

Combined with the successive removal of material by inert gas ion sputtering both techniques are widely used for in-depth profiling through layer stacks to detect e.g. interfacial contamination and interlayer migration. Due to their inherent sensibility to the chemical states of the detected species AES and XPS are indispensable tools for the corroboration of reaction zones.

**X-Ray Fluorescence Spectroscopy (XRF)**

Wavelength-dispersive X-Ray Fluorescence Spectroscopy (XRF) is a non-destructive analytical technique used to identify and determine the concentrations of the elements in solids and liquids. XRF is capable of measuring all elements from beryllium to uranium at trace levels, often below 1ppm, and up to 100%. The composition of the SBT-films has been measured by XRF. X-ray emission is generated by excitation of the sample with X-rays produced from a Rhodium target [Jen74]. The X-rays eject inner-shell electrons and outer-shell electrons take their place and emit X-ray fluorescence photons with a characteristic wavelength depending on the energy difference between outer and inner-shell electron orbitals. The spatial distribution of these characteristic X-rays leaving the sample is isotropic. The line radiations are reflected, according to Bragg’s law, by an analyzing diffraction crystal and pass through a collimator to a Szintillation detector where the energy of the X-ray is converted into electrical impulses or counts. By comparing the intensity of peaks from the measured spectrum with the peaks intensity from similar samples of known composition one can quantify the concentration of the elements in the unknown sample (unit: mass per cm²).


All particles with momentum \( p \) have a de Broglie wavelength \( \lambda \)

\[
\lambda = \frac{h}{p} \quad \text{[eq. 14]}
\]

The wave characteristics of electrons are used in the TEM. TEM cross-sections of the samples are prepared by mechanical grinding and argon ion milling. The difference in electron scattering, passing
tough the thinned sample gives the image. Typically, a 1nm electron beam from a field emission gun with 100-200keV accelerating voltage is used. The resolution is about 0.1nm. Also, Energy Dispersive X-ray (EDX) or Electron Energy Loss Spectroscopy (EELS) analysis can be carried out in a TEM to obtain information about the chemical nature of the species.

**Secondary Ion Mass Spectroscopy (SIMS)**

In SIMS analysis, the ions sputtered off the surface of a sample are analyzed using a mass spectrometer. A primary beam of Cs⁺, O₂⁺, or O⁻ is used to ion mill material from the surface, and mass analysis is then carried out on the ions that have been sputtered off. The depth of profile is generated in a fashion similar to that of Auger analysis coupled with ion milling.

**Pull Test**

The pull test is a quantitative measurement method for the adhesion between substrate and thin films [Bic98]. It consists of a pull stud bonded perpendicular to the film surface with heat curable epoxy glue. The bonding area was \( \pi \cdot (1/2 \cdot 2.7\text{mm})^2 = 5.7\text{mm}^2 \), and the cure condition was 120°C for 30min. The film was then continuously pulled up to 100MPa or until the film was removed from the Si (Figure 18). The force was detected automatically immediately after peeling and given in units of kg/cm². The disadvantage of the pull test method is that the results are dependent on the quality of the glue, and the fact that several interfaces are put under tensile stress. This results in a large scatter of the test results. Therefore, for each sample about 6-10 measurements were made. The error bars were usually in the 20% range. Also, due to systematic errors (baking temperature for the glue, person the measurement made, ...), only one set of samples measured from one person within a few hours is compared to another set of sample.
4. Effects of Pt/Ti electrode on microstructural and electrical properties of SBT thin films

4.1. Introduction

Ferroelectric materials like SrBi$_2$Ta$_2$O$_9$ (SBT) and Pb(Zr,Ti)O$_3$ (PZT) are investigated for capacitor material used in nonvolatile Ferroelectric Random-Access Memories. SBT is favored because of its low voltage and excellent fatigue properties on platinum electrodes [Ara95] [Ama95] [Auc98]. Pt is the electrode material of choice due to its high stability against oxidation and its chemical inertness. However, exactly these properties make it hard to etch and are responsible for adhesion issues. Pt hardly reacts with the most commonly used SiO$_2$ interlayer dielectric (ILD) in semiconductor industry leading to poor adhesion of Pt electrodes on SiO$_2$. This is valid for both interfaces of the Pt bottom electrode and Pt top electrode since SiO$_2$ is used as ILD for all metal levels. Therefore an adhesion promoter is used. For test structures or low-density applications with the offset memory cell (see figure 11 on page 24), Ti is mostly used. However, there are several issues by using Ti. It is known that the titanium layer is diffusing inside the platinum and even to its surface during annealing [Bru91] [Sha93] [Kan99] [Sch97]. Titanium inside and underneath the platinum is oxidized during annealing in O$_2$. This leads to degradation of the adhesion, formation of hillocks, increase of stress and altered electrical properties of the ferroelectric capacitors [Deh99] [Nas98] [Kan99] [Sch97].

Using Pt electrodes on TiO$_x$ or IrO$_x$ gives different electrical results. It is reported [Sch97] that by using Pt/TiO$_x$ electrodes higher polarization values are obtained. This was attributed to the suppressed diffusion of titanium inside the platinum layer. To reduce Ti diffusion, the use of larger Pt grains by Pt deposition at temperatures above 300°C has also been proposed [Nas98]. However, it is not clear how a reduction of Ti diffusion would affect the electrical properties. By means of Rutherford backscattering analysis (RBS) and Heavy Ion Elastic Recoil Detection Analysis (HIERDA) evidence of diffusion of bismuth through the platinum bottom electrode was reported [Sta96] but not correlated to electrical results. In this chapter Pt/Ti and Pt/TiO$_x$ electrodes, and the influence of Ti on SBT will be studied. Microstructural and electrical properties will be given. The incorporation of Ti inside the SBT film by doping of SBT with Ti will be discussed. In this way the impact of Ti on the electrical properties of SBT capacitors becomes clear. Also, the formation of interfacial layers by diffusion will be evaluated. Calculations of the thickness of an assumed interfacial layer using the dielectric constant will help to understand the results observed. By calculating the Bi loss (ratio of bismuth content after wet chemical etching of SBT layer on Pt electrode and bismuth content after SBT coating and crystallization anneal) using the Total XRay Fluorescence (TXRF) technique, the difference in electrical properties of Pt/Ti versus Pt/TiO$_x$ electrodes can be...
attributed to the formation of a Bi deficient interfacial layer and the suppressed grain growth of SBT due to the loss of bismuth into the Pt bottom electrode.

4.2. Characterization of planar Pt/Ti electrodes and the Pt/SBT/Pt module

4.2.1. Interdiffusion of Ti layer in the Pt/Ti bottom electrode

The Pt/SBT/Pt/Ti/SiO$_2$ capacitor module consists of the Pt/Ti bottom electrode, the SBT film and the Pt top electrode. Each process step is followed by an anneal in oxygen (see chapter 3.1).

In figure 19 SEM cross section pictures of Pt/Ti electrodes after deposition (figure 19a), after annealing at 650°C in O$_2$ (figure 19b), and after SBT coating (figure 19c) plus crystallization anneal at 800°C (figure 19d) are shown. It can be seen that the Ti layer changes its morphology during annealing. There is no distinct titanium layer between Pt and SiO$_2$ anymore after the electrode anneal at 650°C (figure 19b). Therefore, Ti and Pt are interdiffusing. After the crystallization anneal at 800°C a distinctive layer underneath the Pt with grain sizes around 50-100nm is visible (figure 19d). Also, the SEM micrograph shows decorations in the Pt layer with the loss of the columnar structure of the platinum and with inhomogeneous inclusions of secondary grains. Again, the formation of the secondary grains inside the Pt layer indicates that there is some interdiffusion and precipitation within the Pt layer. The secondary grains were measured by TEM (Figure 20). Ti is diffusing mainly along the Pt grain boundaries. Since solubility and diffusion rate of oxygen in bulk Pt are very low [Vel72], oxygen is mainly propagating along the Pt grain boundaries.
Therefore, during annealing in $O_2$, Ti gets oxidized leading to inhomogeneous enclosures of TiO$_x$ along Pt grain boundaries. A volume expansion results due to the difference of the Ti and TiO$_x$ density. Assuming an expansion of Ti only in the z-direction of the wafer and taking the densities and molar masses of Ti and TiO$_x$ (see Figure 10 on page 19) one gets an expansion factor of 1.83 after $O_2$ annealing [eq. 15].

$$N_{n} = \frac{\rho_{n} \cdot V_{n}}{M_{n}} = \frac{\rho_{n} \cdot A \cdot d_{n}}{M_{n}} = N_{TIOx} = \frac{\rho_{TIOx} \cdot A \cdot d_{TIOx}}{M_{TIOx}} \iff \frac{d_{TIOx}}{d_{n}} = \frac{\rho_{n} \cdot M_{TIOx}}{\rho_{TIOx} \cdot M_{n}} = \frac{4.5 \text{ g/cm}^2 \cdot 79.9 \text{ g/mol}}{4.1 \text{ g/cm}^2 \cdot 47.9 \text{ g/mol}} = 1.83 \quad \text{[eq. 15]}$$

Interdiffusion of Ti layer in the Pt/Ti bottom electrode is also seen by AES analysis. In Figure 21 AES curves of SBT/Pt/Ti/SiO$_2$ samples after crystallization anneal at 800°C in $O_2$ with 100nm, 200nm and 300nm platinum electrodes on 10nm titanium and of 200nm platinum on 40nm titanium are shown. For all samples a-d Ti has diffused into the Pt layer and the Ti concentration has a peak just below the Pt surface. The oxygen content follows the Ti curve closely and suggests that Ti is fully oxidized throughout the film. During the electrode anneal Ti diffuses into Pt, where it gets oxidized by $O_2$ diffusing in from the surface.

![Figure 20: TEM picture of Pt/Ti electrode after annealing. Note the diffusion and oxidation of titanium inside the platinum layer.](image)

Once oxidized, the mobility of Ti is greatly reduced. Thus the secondary peak of Ti just below the surface is formed. As the electrode anneal progresses, more oxygen diffuses into the electrode, causing a complete oxidation of Ti. Comparing the AES curves after 650°C electrode anneal and after 800°C crystallization anneal, it is further found that the Ti and corresponding oxygen curves are the same as after SBT coating and annealing [Sch97]. Therefore, once Ti is oxidized no further diffusion of Ti or TiO$_x$ is seen even after additional thermal treatments.
By using high-resolution specular and diffuse X-ray reflectivity (see chapter 3.2 on page 33) as an advanced technique for the characterization of thin films, the interfaces at the nanometer scale can be determined more accurately. For the Pt(100nm)/Ti(10nm) electrode after the 650°C electrode anneal before SBT coating and before the 800°C anneal, a remaining layer of 2.6nm between the Ti and SiO₂ interface was found [Asp01]. This layer is clearly less oxidized than the above-mentioned TiOₓ and not seen in AES.

![Figure 21: AES curves of SBT/Pt/Ti/SiO₂ samples after annealing in O₂ with different electrodes: (a) Pt(100nm)/Ti(20nm), (b) Pt(200nm)/Ti(20nm), (c) Pt(300nm)/Ti(20nm) and (d) Pt(200nm)/Ti(40nm).](image)

To study the influence of the Pt thickness, samples with 100nm, 200nm and 300nm Pt on 20nm Ti are prepared (Figure 21a-c). Also, a sample with 40nm Ti underneath 200nm Pt is prepared (Figure 21d). For
all samples the Ti curves in AES look similar. Ti diffusion inside the Pt layer stops about 50nm underneath the Pt surface independent of the Pt and Ti thickness. Therefore, no Ti is found on top of the Pt layer or inside the SBT film as measured by AES. By assuming that the diffusion of the Ti is mainly determined by the relative diffusion of Ti and O\textsubscript{2} in Pt, different Ti curves as measured by AES and different distances of the Ti to the Pt surface should be obtained for different Ti/Pt thickness. However, the characteristics of the Ti diffusion inside Pt are independent of the Pt and Ti thickness used. Ti diffusion stops 50nm underneath the Pt surface. The thicker the titanium layer the more pronounced is the Ti peak inside the Pt layer (Figure 21d).

Figure 22: (a) Sheet resistance of Pt(200nm)/Ti(20nm) and Pt(200nm) electrodes on SiO\textsubscript{2} for different annealing temperatures. (b) Grain size of a platinum electrode after annealing at different temperatures as measured by AFM.

4.2.2. Sheet resistance of layered Pt bottom electrodes

Measurements of the sheet resistance (see chapter 3.2 on page 34 for details) of the Pt/Ti electrode shown in Figure 22a are consistent with the SEM and AES findings shown above. The sheet resistance is measured after annealing at different temperatures and cooling to RT. After the anneal at 500°C an 18% increase in sheet resistance can be observed for the Pt/Ti electrode. This is most likely due to the diffusion of Ti, and the formation of TiO\textsubscript{2} and a Pt-Ti alloy (see below) in the Pt electrode. After annealing at temperatures higher than 500°C, the sheet resistance drops until it reaches a value slightly below the initial value. Contributing to the drop of the sheet resistance is the crystallization of Pt that causes grain growth (see Figure 22b and Figure 15f on page 27) and a lower resistivity. This effect can be clearly seen on a control wafer, which consisted of a 200nm Pt layer directly on SiO\textsubscript{2} without a titanium layer and underwent an identical annealing cycle (Figure 22a). Here a linear decrease in sheet resistance can be
observed. The final value is 14% lower than that for the Pt/Ti sample, showing the contribution of the TiO$_2$ inclusions to the sheet resistance.

The effect of the Pt sputter temperature on the sheet resistance is shown in Figure 23. Again, due to the grain growth of the platinum electrodes without a Ti layer, a linear decrease of the sheet resistance versus sputter temperature is observed. No difference between Pt/Ti/SiO$_2$ and Pt/SiO$_2$ for temperatures between room temperature and 300°C is seen. However, sputtering the platinum at 550°C leads to an increase in sheet resistance for Pt/Ti/SiO$_2$ whereas for Pt/SiO$_2$ sheet resistance is decreasing further. Since Pt sputtering is done at 4.8\times10^{-3}\text{mbar} in Ar after pumping down to <1\times10^{-7}\text{mbar} before sputtering, formation of TiO$_x$ during sputtering can be neglected. Therefore, the 550°C sputtered Pt/Ti/SiO$_2$ layers consists of a mixture between Ti and Pt due to interdiffusion, resulting in a higher sheet resistance. The formation of a Pt-Ti alloy (i.e. PtTi$_3$) for Pt films sputtered at temperatures >500°C is reported [Eic94].

![Figure 23: Sheet resistance versus sputter temperature of Pt/Ti layer versus Pt only layer.](image)

**4.2.3. Evolution of thin film stress**

Mechanical stress, defined as the force per unit area, plays an important role in studying the physical stability of materials. In the elastic region (no plastic deformation) the stress $\sigma$ is given by Hooke’s law

$$\sigma = E \cdot \epsilon$$  \hspace{1cm} [eq. 16]

where $E$ is the proportionality constant called Young’s modulus and $\epsilon$ the strain. The stress is compressive or tensile if the material under stress will expand or contract, respectively, when the forces causing the stress are eliminated. By convention, compressive stresses are considered negative and tensile stresses are considered positive (see Figure 24). The total stress is the sum of so-called intrinsic stress and the thermal stress.
\[ \sigma = \sigma_{\text{intrinsic}} + \sigma_{\text{thermal}} \]  

[eq. 17]

The intrinsic stress is a function of deposition parameters like temperature, pressure, bias and other equipment configurations. Typically for temperatures \( \leq \frac{1}{3} T_{\text{melting point}} \) intrinsic stresses develop. Engineering the growth process can minimize the intrinsic stress. Thermal stress is a function of the difference in the thermal expansion coefficients of the film \( \alpha_f \) and the substrate \( \alpha_s \)

\[ \sigma_{\text{thermal}} = \frac{E_f}{1-\nu_f} \int_{T_1}^{T_2} (\alpha_{\text{film}} - \alpha_{\text{substrate}}) dT \]  

[eq. 18]

where \( E_f \) is the Young’s modulus and \( \nu = -\varepsilon_\perp / \varepsilon \) the Poisson’s ratio of the film. The value of \( \nu \) is generally close to 1/3 for metals. \( \varepsilon_\perp \) represents the strain in a direction perpendicular to the longitudinal direction along which \( \varepsilon \) is measured. For \( \alpha \) values that are independent of temperature (which is generally not true) one can write

\[ \sigma_{\text{thermal}} = \frac{E_f}{1-\nu_f} (\alpha_{\text{film}} - \alpha_{\text{substrate}})(T_2 - T_1) \]  

[eq. 19]

In Figure 10 on page 19, the \( E/(1-\nu) \) or so-called bulk modulus values and the thermal stress values per degree \( s_{th}/(T_2-T_1) \) for Ti and Pt on Si are summarized.

![Figure 24](image-url)

Figure 24: (a) Evolution of thin film stress during volume expansion like trapping of impurities, ion implantation or oxidation. (b) Evolution of thin film stress during volume contraction like releasing of gas or impurities trapped in the film on annealing at higher temperatures, crystallization or silicide formation.

Reactions at higher temperatures are usually associated with volume changes. Therefore, for films with nonzero intrinsic stress, the effect of temperature anneals on intrinsic stresses can be measured (stress versus temperature measurements). A decrease of stress is seen for thin films with a volume expansion like trapping of impurities, ion implantation or oxidation (Figure 24a). An increase of stress is seen for thin films with a volume contraction like releasing of gas, trapping of impurities in the film during
annealing at higher temperatures, crystallization and silicide formation (Figure 24b). For more information about thin films stress see for instance [Mur93] [Spi95].

In Figure 25 results of residual stress measurements of the Pt electrodes are summarized (see chapter 3.2 on page 35 for measurement details). Residual stress is increasing with deposition temperature of the platinum and becomes tensile if sputtered above 190°C. Pt films sputtered at RT exhibit compressive stress due to volume expansion of trapped Ar atoms from sputtering. The tensile stress for Pt films sputtered above 190°C is generated during cooling due to the difference of the thermal expansion coefficients of Pt and Si. Deposition temperature does no longer have any effect on stress after annealing the samples at 800°C in dry oxygen. All electrodes show almost identical tensile stress of around 0.8 GPa.

Diffusion and oxidation of titanium in Pt/Ti electrodes was investigated by stress-temperature measurements in air using a thin film stress analyzer (see chapter 3.2 on page 35 for measuring details). The curves are compared to Pt only electrodes (Figure 26a). During heating the stress decreases until about 500°C for the Pt/Ti electrode. The reason for that is the higher thermal expansion coefficient of both Ti and Pt compared to the silicon substrate. Literature data for the slopes of stress versus temperature for Ti and Pt (see Figure 10 on page 19) are also shown in Figure 26a, b and c. Since the ratio of the Pt/Ti thickness is 10, the expansion curve of the platinum is overweighing the titanium curve. Therefore, the curve follows the slope of the platinum \( \left( \frac{E_p}{(1-\nu_p)} \right) (\alpha_p - \alpha_{Si}) = 1.77\text{MPa/degree} \). Above about 300°C diffusion and oxidation of the Ti layer starts. This is indicated in the stress temperature plot by a higher slope due to volume expansion. In the same temperature range the pure Pt electrode starts to relax. The relaxation is completed above 600°C for the pure Pt electrode. However, the effect of Ti diffusion and oxidation for the Pt/Ti electrode is stronger and the overall stress becomes more compressive. Above 520°C stress relaxation now occurs even for the Pt/Ti electrode. During the soak time above 700°C only
very minor changes in the stress are observed. This means the stress relaxation is completed. During cooling the layers are still “soft” in the higher temperature regime. Below 400°C the expected slope of the curve for Pt is observed.

Figure 26: (a) Stress-temperature measurements in air of Pt(200nm,190°C)/Ti(20nm) and pure Pt(200nm) electrodes in air. Note the compressive stress beginning at 400°C for the Pt/Ti sample due to the oxidation of Ti. (b) Stress-temperature curves of Pt only electrodes sputtered at RT, 190°C and 500°C. (c) Stress-temperature measurements of Pt(200nm,RT)/Ti(20nm) electrodes in air versus nitrogen. Note the increase in stress beginning at 500°C for the nitrogen-annealed sample due to the formation of a Pt-Ti alloy. (d) Stress versus temperature measurements in air for SBT/Pt/Ti/SiO$_2$ sample. All stress curves shown are aligned to $\sigma=0$ at $T=800°C$.

By comparing the stress-temperature curve of the Pt only electrode sputtered at RT, 190°C and 500°C with the thermal stress expected (Figure 26b), one finds for the threshold temperature of the stress
deviation from the expected curve 80°C, 200°C and 500°C respectively. These values agree with the sputter deposition temperatures.

No reference measurements have been done on the wafers prior to electrode deposition. Therefore, the residual stress value of the film stack on the wafer at the beginning of the heating cycle is not known. All stress temperature curves would start at 0. However, assuming that at 800°C all stress has relaxed, the value at 800°C thus indicates zero stress. Therefore, all stress curves shown in Figure 26 are obtained by aligning or shifting the curves to satisfy $\sigma=0$ for $T=800°C$. After this “alignment” the stress value at the beginning of the heating cycle can be obtained from the graphs. The electrodes sputtered at 190°C are almost under stress free condition (Figure 26a,b) and the electrodes sputtered at RT are under 200MPa of compressive stress (Figure 26c) at the beginning of the heating cycle. These results agree with the stress results shown in Figure 25. During the thermal cycles the layers underwent a stress change of about 1GPa. The stress versus temperature curve of a 2nd temperature cycle is identical to the cooling curve of the 1st cycle. Therefore, no further reactions occur at the second annealing cycle.

Stress-temperature measurements of Pt/Ti electrodes with 100nm, 200nm and 300nm Pt on 10nm Ti show a suppressed increase in compressive stress during Ti diffusion and oxidation between 400°C and 500°C for the thicker platinum electrodes.

Stress-temperature measurements show a quite different behavior for annealing in N$_2$ compared to O$_2$ (Figure 26c). Here a strong tensile stress can be observed between 475°C and 600°C. For the same sample in O$_2$ a strong decrease of stress between 475°C and 600°C is seen due to volume expansion during TiO$_x$ formation. A possible explanation could be the formation of a Pt-Ti alloy (Pt$_3$Ti) or TiN [Kan99] with significant volume reduction leading to an increase of stress for the N$_2$ annealed sample. At higher temperatures the stress generated by this phase transition relaxes and may be compensated by partial oxidation of Ti.

In Figure 26d a stress versus temperature measurement in air for a SBT film on a Pt/Ti/SiO$_2$ substrate is shown. Before the thermal cycle, the SBT layer was amorphous. Therefore, the heating up to 800°C in air should result in crystallization of the SBT. The stress is decreasing linearly with increasing temperature between 200°C and 550°C. From 550°C on up to 800°C, no further decrease of stress is seen. This means in this temperature range SBT is crystallizing since for a identical sample with already crystallized SBT, stress was still decreasing. There is no indication for a phase transition of the ferroelectric SBT during cooling as seen for PZT [Bru98].

From the slope of the stress-temperature curve during cooling of the SBT/Pt/Ti sandwich on SiO$_2$ (1.10MPa/degree), $E_{SBT}(1-\nu_{SBT})((\alpha_{SBT}-\alpha_{Si})$ can be obtained. The total stress $s$ of the films is the mean value of the SBT and Pt stress $s_{SBT}$ and $s_{Pt}$ respectively [Bru98]
\[
\langle \sigma \rangle = \frac{\sigma_{SBT} \cdot d_{SBT} + \sigma_{Pt} \cdot d_{Pt}}{d_{SBT} + d_{Pt}}
\]

where \(d_{SBT}\) and \(d_{Pt}\) are the thicknesses of the SBT and Pt films respectively. Using (eq. 19) for \(s_{SBT}\) and \(s_{Pt}\), the unknown value \([E_{SBT}/(1-\nu_{SBT})](\alpha_{SBT}-\alpha_{Si})\) can be calculated

\[
\langle \sigma \rangle \left( \frac{T_2 - T_1}{T_2 - T_1} \right) = \frac{E_{SBT}(\alpha_{SBT} - \alpha_{Si}) \cdot d_{SBT} + E_{Pt}(\alpha_{Pt} - \alpha_{Si}) \cdot d_{Pt}}{d_{SBT} + d_{Pt}}
\]

Using 1.10MPa/degree for \(<s>/(T_2-T_1)\) (Figure 26d), 1.77MPa/degree for \([E_{Pt}/(1-\nu_{Pt})](\alpha_{Pt}-\alpha_{Si})\) (see Figure 10 on page 19) and 200nm for \(d_{Pt}\) and 180nm for \(d_{SBT}\), the value \([E_{SBT}/(1-\nu_{SBT})](\alpha_{SBT}-\alpha_{Si}) = 0.36MPa/degree\) is obtained. Assuming the following values (Young’s modulus of SBT \(E_{SBT}=72GPa\) for polycrystalline unpoled material [Coo63], Poisson ratio of SBT \(\nu_{SBT}=0.3\) and \(\alpha_{Si}=2.6 \times 10^{-6}K^{-1}\), the thermal expansion coefficient of SBT is obtained as \(\alpha_{SBT}=6.1 \times 10^{-6}K^{-1}\).

4.2.4. Hillock formation on Pt bottom and top electrodes

Processing of ferroelectric has been complicated by Pt hillock formation, small outgrowths on the film, during annealing. This morphology change, which results in a rough electrode surface and shorted capacitors, has been studied by several groups [Eic94] [Spi92][Mat98][Eri91]. It is found that hillock formation depends on deposition technique (e.g. sputtering, e-beam evaporation), thickness, deposition temperature and the substrate used (e.g. Ti/SiO\(_2\) versus SiO\(_2\) only). This complicated behavior may account for the different results reported about hillock formation. Therefore, minimizing hillock formation must be optimized for each specific tool environment and processes. In order to study the formation of Pt hillocks, Pt electrodes are used without the Ti adhesion layer.

In Figure 27a the hillock densities of 100nm and 200nm platinum layers sputtered at 190°C are shown\(^3\). For both electrodes, hillock densities are increasing after annealing between 400°C-600°C and cooling to RT. As shown in Figure 26a for the platinum electrode without a Ti layer, compressive stress reaches its maximum values at 400°C before relaxing between 400°C and 600°C. This means, the compressive stress relaxes because the Pt film cannot hold the strain as the temperature is increased and the stress is released by the formation of hillocks. This supports a stress relief process that gives rise to the hillock formation. Between RT and 200 the stress-temperature curve of the Pt electrode sputtered at 190°C (Figure 26a) follows exactly the expected Pt curve. Above 200°C stress is now decreasing slower than the expected thermal stress of platinum. This is due to the volume shrinkage during Pt crystallization since below 400°C no significant increase in hillock density is seen (Figure 27a). At 400°C stress starts to increase

\(^3\) Density of hillocks was determined from SEM and optical microscope after cooling to RT. The area of hillock was determined by SEM only.
(stress relief) again due to further Pt crystallization but this time also due to the formation of hillocks since between 400°C and 600°C the highest density of hillocks is observed (Figure 27a).

![Graphs](image)

Figure 27: (a) Hillock density and (b) area of hillock as a function of Pt bottom electrode thickness and anneal temperature. (c) Pt electrode thickness versus annealing temperature illustrating where hillocks are seen. The dotted line is a assumption for the critical temperature separating a hillock-free region from a region where hillocks are observed.

The highest number of hillock density is seen for the 200nm Pt electrode (Figure 27a). Also, the area of the hillocks is larger for the 200nm Pt electrode (Figure 27b). This is due to the ability of a thicker film to transport atoms along grain boundaries to a much larger extent than in a thin film in proportion to the size of the Pt grain in the film [Eri91]. Therefore, to produce the same atomic flow to the hillock, a higher diffusion coefficient of the atoms along the grain boundaries or a higher temperature are needed compared
to a thicker film. At elevated temperatures, the density of the hillocks is decreasing for both the 100nm as well as the 200nm electrode. Although the density of the hillocks versus annealing temperature is decreasing for the 100nm and the 200nm electrode, the area of the hillock is not decreasing up to 800°C for the 200nm electrode but does for the 100nm electrode. This suggests that to decrease the area of the hillock on a 200nm electrode, temperatures above 800°C may be necessary.

In Figure 27c the thickness of the Pt electrode versus annealing temperature is plotted showing if at a certain thickness-temperature combination hillocks are seen. The dotted line is an assumption for the critical temperature at which hillocks will occur or disappear for a certain Pt thickness.

It is observed that sputtering the platinum at 550°C gives hillock free layers after deposition and after annealing at any temperature. This is valid for both 100nm and 200nm platinum electrodes. Therefore, for Pt films sputtered at higher temperatures than 190°C the dotted line in Figure 27c shifts upwards to thicker Pt films. The hillock-free condition at any annealing temperature for Pt films sputtered at 550°C can be explained by the stress-temperature curve for these Pt films. The stress-temperature curve for platinum sputtered at 500°C follows the expected thermal stress curve of platinum and does not show any stress relaxation up to 500°C (see Figure 26b). Since hillock growth is mainly seen between 400°C and 600°C during compressive stress relief, hillock formation is only minor for 550°C deposited platinum films. Therefore, annealing the 550°C sputtered platinum films, no hillocks are formed.

Hillocks can also be seen on platinum top electrodes. For Pt/SBT/SiO₂ structures without a bottom electrode as used for 3D integration (see chapter 2.5), hillocks are seen on the top electrode (Figure 28a,b). Therefore, the interface between the platinum layer and the substrate is important for the growth of the hillocks. It is also worth to note, that common for all hillocks in the films annealed at high temperatures is that they are completely integrated with the film material beneath them. No clear line between hillock on top of the surface and the film material beneath it can be seen. No hillocks are usually seen on Pt top electrodes for Pt/SBT/Pt structures with a Pt bottom electrode underneath the SBT.

Though much remains to be done, a consensus seems to exist to the general principles behind the formation of hillocks. Thus, hillocks are formed under the influence of compressive stress at elevated temperatures. Both the size and the number of the hillocks increase with increasing film thickness. The growth of a hillock involves a transport of atoms along grain boundaries and, possibly, along the film surface as well as the interface between film and substrate. Furthermore, an hillock is formed during the early heating stage of an annealing cycle. At higher annealing temperatures, less Pt hillocks are observed. The critical parameters identified are: sputter deposition temperature, thickness, annealing temperature and the substrate used.
4.2.5. **Adhesion characteristics**

As already discussed above, Pt is the favored electrode material for ferroelectric thin films because of its stability in high-temperature oxidizing atmospheres. However, adhesion of Pt on SiO$_2$ is poor. To achieve high adhesion, a strong interatomic bonding across the film-substrate interface and a low level of film stress is necessary. Adhesion is a result of "physical bonding" (van der Waal forces, adsorption) or even better "chemical bonding" (chemisorption). For improving the adhesion of the platinum to the substrate, Ti is used frequently.

To study the adhesion the adhesive tape test [Lee96], the pull test [Kon92] and the scratch test [Kan99] can be used. In this study the adhesion properties of the films were evaluated by the pull test method (see chapter 3.2 on page 38).

In Figure 29a the adhesion values for Pt/Ti electrodes on SiO$_2$ with 0nm, 10nm and 20nm Ti are shown (no anneal was performed). Without Ti as adhesion promoter the Al studs on the Pt electrodes fall off already without performing the actual pull test. Increasing the Ti thickness improves the adhesive strength remarkably. It is believed that the increase of the surface energy is directly related to the adhesion and the wetting property [Kin88]. Therefore, the Ti layer is effective for improving the Pt wetting property, which is equivalent to the improvement of the adhesion. An extreme case of very poor wetting characteristics of Pt on SiO$_2$ without Ti layer is shown in Figure 32 after annealing at 800°C in O$_2$.

It is well known that Ti very easily forms silicides with silicon. Therefore, TiSi$_x$ formation between Ti and SiO$_2$, which could quite possible be responsible for improving the adhesion between Pt and SiO$_2$, was examined by XPS. However, no indication was found for both TiSi$_x$ as well as PtSi$_x$ formation for as deposited films and films annealed at 650°C in O$_2$. 

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Figure 28: (a) SEM picture of a Pt hillock on the top electrode. (b) Cross section SEM of a Pt hillock on the top electrode.
In Figure 29b the adhesion of the Pt/TiO$_x$/SiO$_2$ electrode system is shown. Here Ti was oxidized in the RTP at 700°C for 5 min in O$_2$ before deposition of Pt. Up to 400°C adhesion was always above 700 kg/cm$^2$. However, for samples annealed between 500°C and 800°C adhesion drops to 300 kg/cm$^2$.

Figure 29: (a) Adhesion of Pt/Ti electrodes on SiO$_2$ for different Ti thickness. (b) Adhesion of Pt/TiO$_x$ electrodes on SiO$_2$ for different annealing temperatures.

Much better adhesion is expected for the Pt/Ti/SiO$_2$ electrode. In Figure 30a the adhesion of Pt/Ti bottom electrodes are shown. Sputter temperature for Pt was 190°C and 550°C, and sputter temperature for Ti was 450°C for all samples$^4$. For the 190°C deposited Pt samples, best adhesion is obtained after pre-annealing at 400°C and 500°C. Without pre-annealing the lack of interdiffusion of Ti and Pt (see Figure 19a) leads to poor adhesion. At temperatures $>$400°C Ti diffuses into the Pt (see Figure 26a) and no Ti layer is visible anymore. The critical temperature range for the Ti to diffuse and to oxidize was found to be between 400°C and 600°C. Since this temperature range coincides with the improvement of the adhesion characteristics for the Pt/Ti electrode sputtered at 190°C, the interdiffusion of Ti and Pt and the formation of TiO$_x$ between 400°C and 600°C is assumed to improve the adhesion. For the samples annealed at 650°C, 700°C and 800°C adhesion drops to 300 kg/cm$^2$. This can be understood in terms of a well-defined, crystallized and brittle TiO$_x$ layer underneath the Pt (see Figure 19d). After crystallization of the TiO$_x$ layer underneath the Pt, the Pt layer now looks more porous with inhomogeneous incorporation of TiO$_x$ inside the Pt. Therefore, adhesion degradation after high temperature annealing in O$_2$ is attributed to the depletion of the Ti adhesion layer and to the large internal stress due to crystallization and grain growth of Pt and brittle TiO$_x$ layers.

$^4$ No influence of the Ti sputter temperature on adhesion was found.
For the 550°C sputtered Pt film, very good adhesion is already obtained without any annealing at all (Figure 30a). Also, after annealing at 650°C adhesion of the 550°C sputtered Pt/Ti film is superior compared to the 190°C sputtered Pt/Ti film. The main reason for this different behavior is the fact that sputtering at 550°C already promotes Ti diffusion during sputtering which results in the formation of a Pt-Ti alloy. In consequence, a better adhesion should be obtained. In chapter 4.2.4 it was also shown that the 550°C sputtered Pt films did not show any hillock formation due to missing stress relaxation up to 550°C. This overall smaller change of stress for the 550°C sputtered Pt film could also quite possibly result in a better adhesive strength. By high-resolution specular x-ray reflectivity study under grazing angles (see chapter 4.2.1 on page 33) it could also be shown that for the Pt/Ti/SiO$_2$ sample sputtered at 550°C and annealed at 650°C, at the SiO$_2$ interface a relatively weakly oxidized, remaining Ti-layer of about 2nm remained [Asp01]. This remaining Ti layer explains why the adhesion is still about 800kg/cm$^2$ [Nas98].

Increasing the annealing temperature further, adhesion also decreases although the adhesion for the 550°C sputtered Pt films is still better than for the 190°C sputtered film. Again, the formation of a well defined, crystallized and brittle TiO$_x$ layer underneath the Pt at 800°C is responsible for the loss of adhesion.

Comparing the adhesion of the Pt/Ti electrode (Figure 30a) with the Pt/TiO$_x$ electrode (Figure 29b) sputtered at 550°C the following result is obtained. The adhesion of Pt/Ti is superior compared to Pt/TiO$_x$ if annealed at 500°C and 650°C whereas the samples not annealed at all, annealed below 500°C and annealed at 800°C show only minor differences.

In Figure 30b the adhesion values for Pt/Ti electrodes on SiO$_2$ with 100nm, 200nm and 300nm Pt are shown. While increasing the platinum thickness at constant Ti thickness, only little dependency on the adhesion is observed. Annealing these samples at 800°C again results in a much more drastic effect.
Adhesive strength of 400kg/cm² is measured after annealing at 800°C irrespective of the platinum thickness used.

![Diagram](image)

Figure 31: Pull test of the entire Pt/SBT/Pt/Ti stack: (a) after top electrode deposition and (b) after post anneal. For the non-annealed sample peeling is mainly observed at the interface between SBT and bottom electrode whereas after post annealing peeling occurs mainly at the interface between top electrode and SBT.

![SEM Image](image)

Figure 32: SEM picture of a thin Pt layer on SiO₂ after annealing at 800°C in O₂. The appearance of dark Pt areas is due to charging of isolated Pt features.

Adhesion tests were also performed on SBT/Pt/Ti/SiO₂ samples. Two sets of samples after SBT coating and RTP bake at 725°C for 30s in O₂, and after crystallization anneal at 800°C for 1h in O₂ are compared. The same rule as above for the Pt/Ti electrodes holds: the higher the temperature budget the lower the adhesion. The adhesive force decreased from 600±100kg/cm² after SBT coating and RTP bake to 350±100kg/cm² after crystallization. The crystallization or grain growth of the SBT and Pt layers at higher temperatures leads to porosity and therefore weakens the adhesive strength (see Figure 19d).

The adhesive strength of the entire Pt/SBT/Pt/Ti/SiO₂ stack after top electrode deposition is 420±80kg/cm² and 490±100kg/cm² after post anneal at 800°C. There is only a slight difference between these values. However, a remarkable difference is seen at the interface where it peeled off. For the non-annealed Pt/SBT/Pt/Ti/SiO₂ sample peeling is mainly observed at the interface between SBT and bottom electrode (Figure 31a) whereas after post annealing peeling occurs mainly at the interface between top electrode and SBT (Figure 31b). Therefore, the crystallization of the Pt top electrode leads to a lower adhesive strength.

The adhesion of the SiO₂ interlayer dielectric (ILD) on the entire Pt/SBT/Pt stack is very poor. To improve the adhesion, plasma pretreatment [Har00d] or the introduction of additional adhesion layers above the Pt top electrode like Ti, WSi₆, TaN, IrOₓ, ... can be introduced [Har00e]. An insitu O₃ RF treatment for 30s at 500W results not only in cleaning the surface but also in activation of Pt surface atoms due to the RF treatment. The surface activated by the plasma treatment will increase its bondability with the atoms of the following insitu deposited SiO₂ layer. From the additional adhesion layers stated above, WSi₆ was found
to be the best glue layer. However, due to heavy interdiffusion of WSi, and Pt, formation of PtSi, and Pt-W alloy, and diffusion of Si even to the Pt/SBT interface, very low polarization values are obtained.

4.3. Electrical results and microstructural properties of SBT capacitors with Pt/Ti electrodes

4.3.1. Variation of the Pt/Ti electrodes

To study the influence of the Pt/Ti bottom electrode, the electrical properties of the Pt/SBT/Pt/Ti capacitors with different Pt/Ti bottom electrodes were studied. In Figure 33b the electrical data of SBT capacitors with Pt(50nm)/Ti(10nm), Pt(100nm)/Ti(10nm) and Pt(200nm)/Ti(10nm) electrodes are shown.

| electrode         | polarization [µC/cm²] | coercive voltage [V] | leakage current [A/cm²] | dielectric constant | ε |
|-------------------|-----------------------|-----------------------|-------------------------|---------------------|--|---|
| A                 | 12.3                  | 1.29                  | 1.2E-7                  | 276                 |   |   |
| B                 | (17.7)                | 2.11                  | 5.5E-5                  | 225                 |   |   |
| C                 | (11.9)                | 2.31                  | 3.8E-5                  | 200                 |   |   |

| electrode         | polarization [µC/cm²] | coercive voltage [V] | leakage current [A/cm²] | dielectric constant | ε |
|-------------------|-----------------------|-----------------------|-------------------------|---------------------|--|---|
| A                 | 15.9                  | 1.20                  | 1.7E-7                  | 225                 |   |   |
| B                 | 12.5                  | 1.29                  | 9.2E-8                  | 225                 |   |   |
| C                 | (14.1)                | 1.93                  | 2.3E-5                  | 200                 |   |   |

Figure 33: P-V hysteresis loops and electrical results of SBT thin films deposited on Pt/Ti electrodes with (a) different Ti thickness and (b) different Pt thickness.

Highest value of the remanent polarization, lowest value for the coercive voltage and low leakage current are obtained with the Pt(200nm)/Ti(10nm) electrode. High values for the leakage current and coercive voltage are seen for the Pt(50nm)/Ti(10nm) electrode. The electrical results of increasing the Ti thickness while keeping the Pt thickness constant are shown in Figure 33a. For the Pt/(100nm)/Ti(20nm) electrode, the leakage current is 2 orders of magnitude higher, the $2V_c$ value is almost double and the dielectric
constant is 19% lower compared to the Pt(100nm)/Ti(10nm) electrode. Increasing the Ti thickness even to 40nm leads to further decrease of the dielectric constant and increase of coercive voltage $2V_c$.

Therefore, by using Pt/Ti bottom electrodes the following statement is valid: the thicker the Pt bottom electrodes or the thinner the Ti layer (small Ti/Pt ratio) the lower the leakage currents, the lower the $2V_c$ values and the higher the $2P_r$ values. However due to hillock formation more shorts are seen on 200nm Pt bottom electrodes compared to 100nm (see chapter 4.2.4).

![Figure 34: (a) SEM cross-section of a Pt/SBT/Pt/TiO$_2$/SiO$_2$/Si stack after all anneals. The TiO$_2$ and Pt layers in the bottom electrode are clearly separated and there are no TiO$_2$ inclusions in the Pt film. (b) AES result of a Pt/SBT/Pt/TiO$_x$/SiO$_2$ sample shows no interdiffusion of Ti after all anneals.](image)

Ti diffusion can be suppressed by forming TiO$_2$ before the Pt deposition. In this experiment, the Ti layer was oxidized at 700°C in O$_2$ before the Pt layer was deposited. SEM micrographs show no indication for TiO$_2$ inclusions inside the Pt layer (Figure 34a). The SBT film looks dense and crystalline. No diffusion of Ti into the Pt layer even for a fully processed sample after all anneals is seen by AES either (Figure 34b).

The absence of Ti inside the Pt bottom electrode by using Pt/TiO$_x$ electrodes significantly enhances the electrical properties of SBT (Figure 35b). $2P_r$ values for the Pt/TiO$_x$ electrodes range from 13 to 19µC/cm$^2$ compared to 12 to 16µC/cm$^2$ for the Pt/Ti electrode. $2V_c$ values range from 1.11 to 1.17V and are always lower than the values for Pt/Ti. Even the Pt(50nm) electrode on TiO$_x$ gives high polarization values and low leakage currents whereas the Pt(50nm) electrode on Ti shows only poor electrical results (Figure 33b).

A simple summary of the electrical data for Pt(50,100,200nm)/Ti(0,10,20,40nm) bottom electrodes is shown in Table 2. A cross marks bottom electrode combinations that give only poor results.
Figure 35: Electrical results and P-V hysteresis loops of SBT thin films deposited on (a) Pt/Pt/Ti, Pt/Ti and Ti/Pt/Ti, and (b) on Pt/Ti and Pt/TiOx electrodes with different Pt thickness.

<table>
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<th>2Vc @ 5V [V]</th>
<th>IL @ 2V [A/cm²]</th>
<th>dielectric constant ε</th>
</tr>
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<td>1.20</td>
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<td>C</td>
<td>3.6</td>
<td>1.38</td>
<td>1.6E-6</td>
<td>192</td>
</tr>
</tbody>
</table>

Table 2: Summary of the electrical results. A cross marks bottom electrode combinations with poor results.

Figure 36: Electrical results Pt/SBT/Pt/Ti capacitors with Pt bottom electrode sputtered at 60°C, 190°C, 300°C and 550°C.
Figure 37: (a) SEM cross-section of a Pt/SBT/Ti/Pt/Ti/SiO$_2$ sample after all anneals. Both SBT and Pt films are very porous. (b) AES result of a Pt/SBT/Ti/Pt/Ti/SiO$_2$ sample shows Ti throughout the thickness of the SBT and Pt film after all anneals.

Figure 38: 2Pr values at constant electric field versus film thickness for SBT on Pt/TiO$_x$ versus Pt/Ti.

By introducing an additional 50nm Pt layer on top of a pre annealed Pt/Ti electrode, higher polarization, lower coercive voltage, same leakage current and higher dielectric constant compared to the Pt(100nm)/Ti(10nm) electrode are obtained (curve A versus B in Figure 35a). To study the direct influence of Ti on SBT properties, a 5nm Ti layer on top of a pre annealed Pt/Ti electrode was used before SBT coating. After SBT coating and crystallization, Ti is found throughout the thickness of the SBT film (see AES in Figure 37b). The SEM of the annealed Pt/SBT/TiO$_x$/Pt/TiO$_x$/SiO$_2$ sample (Figure 37a) reveals, that both SBT and Pt films get very porous and finely grained. For this sample only poor electrical properties are obtained (curve C in Figure 35a), stressing the negative impact of Ti on SBT. The formation
of a thin TiO$_x$ interfacial layer between bottom electrode and SBT as well as the reaction of SBT and Ti has to be considered here.

As seen in Figure 36 higher polarization values are obtained for Pt bottom electrode sputtered at 550°C. Sputtering the Pt at 300°C or RT does not alter the electrical properties (see also [Nas98]).

In Figure 38 remanent polarization versus SBT film thickness is shown for Pt/TiO$_x$ and Pt/Ti electrodes. Again about 30% higher polarization values are achieved on Pt/TiO$_x$ electrodes compared to Pt/Ti electrodes. Also, polarization values for thinner SBT films do not tend to decrease for Pt/TiO$_x$ electrodes as for Pt/Ti electrodes.

4.3.2. Ti doping of SBT

As shown above, whenever electrodes with a high ratio of Ti thickness versus Pt thickness were used, poor electrical data were obtained. These results demonstrate the negative effect of Ti in the bottom electrode on the characteristics of the Pt/SBT/Pt/Ti capacitors. In order to study the direct influence of Ti on the electrical properties of SBT capacitors, doping experiments of SBT with Ti were performed.

Doping experiments of SBT with Ti were done by mixing SBT MOD solution with TiO$_x$ solution. The solutions used are 0.2m SBT in n-octane and 0.6m TiO$_x$. Further dilution was done with n-butylacetate. Due to thickness adjustments of SBT during spin coating, the preferred dilution for SBT is 0.12m. 100% Ti content in SBT means 0.12 molar Ti solution was mixed with 0.12 molar SBT solution. In other words, SBT and Ti is mixed with identical molarity in the total volume. 50% doping means Ti is mixed with half the molarity of SBT in the total volume. According to the following equations [eq. 22] all solutions for $X=0.001\%$, 0.01%, 0.1%, 1%, 10%, 50% and 100% Ti-doping of SBT are mixed.

<table>
<thead>
<tr>
<th>Ti-doping n</th>
<th>Volume SBT$^{0.2m}$</th>
<th>Volume TiO$_x^{0.6m}$</th>
<th>Volume n-butylacetate</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X/100 V</td>
<td>1/3·n·V</td>
<td>(2/3 - 1/3·n)·V</td>
</tr>
</tbody>
</table>

For verification of the equations above, the Ti-molarity in the used total volume [eq. 23] should equal n times the SBT-molarity in the used total volume [eq. 24].

$$\text{Ti-molarity} = \frac{\text{volume TiO}_x}{\text{total volume}} = 0.6m = \frac{1/3·n·V}{V + 1/3·n·V + (2/3 - 1/3·n)·V} \cdot 0.6m = \frac{3}{25} m \cdot n = 0.12m \cdot n$$  \[eq. 23\]

$$\text{SBT-molarity} = \frac{\text{volume SBT}}{\text{total volume}} = 0.2m = \frac{V}{V + 1/3·n·V + (2/3 - 1/3·n)·V} \cdot 0.2m = \frac{3}{25} m = 0.12m$$  \[eq. 24\]

The corresponding electrical results, hysteresis loops, polarization and dielectric constant values of 0, 0.001%, 0.01%, 0.1%, 1%, 10%, 50% and 100% Ti-doped SBT are shown in Figure 39a-d respectively. No degradation of 2P, and 2$V_c$ values up to 1% doping with Ti is observed. However, leakage currents are
slightly increased compared to the Ti free SBT sample. Further increase of the Ti content leads to a decrease of the leakage current. For 10% Ti content and higher, polarization values decrease significantly and hysteresis loops become paraelectric. Highest coercive voltages are measured for 10% and 50% Ti content. Due to paraelectric shape of hysteresis loops coercive voltage is lowest for 100% Ti. For the dielectric constant versus Ti content a similar behavior as for the polarization is obtained. No change up to 10% Ti is seen for the dielectric constant whereas for 100% Ti the dielectric constant drops to 95.

<table>
<thead>
<tr>
<th>Ti content [%]</th>
<th>2Pr @ 5V [µC/cm²]</th>
<th>2Vc @ 5V [V]</th>
<th>IL @ 2V [A/cm²]</th>
<th>ε [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>12,9</td>
<td>1,24</td>
<td>1,0E-7</td>
<td>297</td>
</tr>
<tr>
<td>0,001</td>
<td>13,1</td>
<td>1,26</td>
<td>5,6E-7</td>
<td>313</td>
</tr>
<tr>
<td>0,01</td>
<td>13,6</td>
<td>1,21</td>
<td>4,4E-7</td>
<td>318</td>
</tr>
<tr>
<td>0,1</td>
<td>12,7</td>
<td>1,28</td>
<td>2,4E-7</td>
<td>293</td>
</tr>
<tr>
<td>1</td>
<td>12,9</td>
<td>1,26</td>
<td>1,6E-7</td>
<td>304</td>
</tr>
<tr>
<td>10</td>
<td>9,2</td>
<td>1,56</td>
<td>2,8E-8</td>
<td>164</td>
</tr>
<tr>
<td>50</td>
<td>2,6</td>
<td>1,7</td>
<td>2,8E-8</td>
<td>164</td>
</tr>
<tr>
<td>100</td>
<td>0,4</td>
<td>0,78</td>
<td>1,9E-8</td>
<td>95</td>
</tr>
</tbody>
</table>

Figure 39: (a) All electrical results, (b) P-V hysteresis loops, (c) polarization and (d) dielectric constant values of SBT thin films versus different Ti content. All data shown originate from two different lots, as indicated by different symbols in c) and d).
4.3.3. **Loss of Bi into Pt/Ti, Pt/TiO$_x$, and Pt/IrO$_x$ electrode**

In Figure 40a a TEM cross section of a SBT/Pt/Ti sample after crystallization anneal is shown. The bright areas between SBT/Pt and Pt/Ti are a result of adhesion failures during TEM preparation and do not show additional interfacial layers. In Figure 40b the corresponding EDX data of the Ti-area underneath the platinum marked “8” in the TEM picture are shown. Besides the main elements titanium and oxygen, bismuth is found. The original Ti-layer has reacted to Bi-Ti-oxide as can be seen from the EDX spectrum. Bi-M, Bi-L, Ti-K and O-K lines show up strongly. This means, during annealing of the SBT layer, bismuth is diffusing inside and through the platinum layer to react with Ti to BTO (BiTi$_x$O$_y$). For determination of the ratio of bismuth diffused inside and through the platinum bottom electrode, the XRF technique is used (see chapter 3.2 on page 37).

Three types of layered electrodes are used: Pt/Ti, Pt/TiO$_x$ and Pt/IrO$_x$. At first, the content of bismuth after SBT coating and crystallization anneal is measured by XRF on SBT/Pt/Ti, SBT/Pt/TiO$_x$, and SBT/Pt/IrO$_x$. After etching off the SBT film using a HF/HNO$_3$-based solution, the content of bismuth is again measured by XRF on Pt/Ti, Pt/TiO$_x$, and Pt/IrO$_x$. The ratio of bismuth after wet chemical etching of the SBT layer and after SBT coating and crystallization anneal gives the loss of bismuth to the bottom electrode. In Figure 41 all values for the different electrodes are summarized. It can be seen that lowest values are

---

5 As a sanity check of the efficiency of the wet etching chemistry, XRF measurements after etching off the SBT layer are performed to check for Ta, Sr and Bi. No Sr and Ta is measured on all platinum electrodes.
obtained for the Pt/TiO$_x$ and Pt/IrO$_x$ electrodes. For the Pt/Ti electrode the loss of bismuth is almost 40% higher compared to Pt/TiO$_x$ and Pt/IrO$_x$ electrodes.

<table>
<thead>
<tr>
<th></th>
<th>Bi before SBT etch [µg/cm²]</th>
<th>Bi after SBT etch [µg/cm²]</th>
<th>Bi loss ratio average [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBT/Pt 100nm / Ti</td>
<td>51.08</td>
<td>2.59</td>
<td>5.07</td>
</tr>
<tr>
<td>SBT/Pt 100nm / TiO$_x$</td>
<td>50.72</td>
<td>2.29</td>
<td>4.51</td>
</tr>
<tr>
<td>SBT/Pt 200nm / Ti</td>
<td>50.76</td>
<td>2.23</td>
<td>4.39</td>
</tr>
<tr>
<td>SBT/Pt 100nm / TiO$_x$</td>
<td>51.39</td>
<td>1.98</td>
<td>3.85</td>
</tr>
<tr>
<td>SBT/Pt 200nm / TiO$_x$</td>
<td>51.04</td>
<td>1.56</td>
<td>3.06</td>
</tr>
<tr>
<td>SBT/Pt 50nm / IrO$_x$</td>
<td>51.21</td>
<td>1.67</td>
<td>3.26</td>
</tr>
<tr>
<td>SBT/Pt 100nm / IrO$_x$</td>
<td>51.85</td>
<td>1.83</td>
<td>3.53</td>
</tr>
<tr>
<td>SBT/Pt 200nm / IrO$_x$</td>
<td>51.16</td>
<td>1.68</td>
<td>3.28</td>
</tr>
<tr>
<td>SBT / SiN</td>
<td>53.3</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 41: Results of XRF measurements to determine the loss of bismuth into Pt/Ti, Pt/TiO$_x$ and Pt/IrO$_x$ electrodes.

4.3.4. Interfacial layer and discussion

Incorporation of Ti

Small amounts of Ti did not influence the ferroelectric properties. Large amounts of Ti (≥10%) lead to degradation of the ferroelectric properties very likely due to the formation of TiO$_x$ and BiTiO$_x$. Small amounts of Ti inside the SBT caused only slight differences in the electrical characteristics of the capacitors. To explain the differences between the electrical data of Pt/Ti and Pt/TiO$_x$ bottom electrodes by the possible incorporation of Ti inside the SBT film, Ti content in the SBT film should be at least 10%. However, no diffusion of Ti on top of Pt or inside SBT was seen by AES. Therefore, the incorporation of Ti inside the SBT layer seems not to be the root cause for the lower polarization values by using Pt/Ti electrodes versus Pt/TiO$_x$ electrodes.

Interfacial layer and loss of bismuth

The average dielectric constant of SBT on Pt/TiO$_x$ electrodes was 339 (see first three values in the table of Figure 42). For all other electrodes used smaller values for the dielectric constant of the SBT films were obtained. An interfacial layer with a dielectric constant significantly lower than 339 would explain this decrease of the dielectric constants by using Pt/Ti electrodes. By assuming two series capacitors (the and no Sr, Ta and Bi is found on SiN (Figure 41). On other wafers it was also shown that the chemistry etches off BiO$_x$. All these results prove the efficiency of the wet etch chemistry.
interfacial layer IL ($\varepsilon_{\text{IL}}$) and the SBT film ($\varepsilon_{\text{SBT}}$) with a total thickness of $d=d_{\text{IL}}+d_{\text{SBT}}$) the thickness $d_{\text{IL}}$ of the interfacial layer can be calculated from the following equation

$$\frac{1}{C} = \frac{1}{C_{\text{IL}}} + \frac{1}{C_{\text{SBT}}} \iff \frac{d}{\varepsilon_{\text{A}}\varepsilon_{\text{A}}} = \frac{d_{\text{IL}}}{\varepsilon_{\text{A}}\varepsilon_{\text{IL}}} + \frac{d_{\text{SBT}}}{\varepsilon_{\text{A}}\varepsilon_{\text{SBT}}} \iff d_{\text{IL}} = \frac{\varepsilon_{\text{IL}}(\varepsilon_{\text{SBT}} - \varepsilon_{\text{A}})}{\varepsilon_{\text{SBT}} - \varepsilon_{\text{IL}}}.d$$  \hspace{1cm} [eq. 25]

By plotting the calculated values of $d_{\text{IL}}$ versus the ratio Ti/Pt of the electrode thickness for different assumed values of the dielectric constant of IL, an almost linear relationship is obtained (Figure 42).

<table>
<thead>
<tr>
<th>$d_{\text{Pt}}$ [nm]</th>
<th>$d_{\text{Ti}}$ [nm]</th>
<th>$d_{\text{Ti}}/d_{\text{Pt}}$</th>
<th>$\varepsilon_{\text{measured}}$</th>
<th>$d_{\text{IL}}$ [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0</td>
<td>0</td>
<td>331</td>
<td>1,1</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
<td>0</td>
<td>343</td>
<td>-0,5</td>
</tr>
<tr>
<td>200</td>
<td>0</td>
<td>0</td>
<td>342</td>
<td>-0,4</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
<td>0,1</td>
<td>276</td>
<td>10,3</td>
</tr>
<tr>
<td>100</td>
<td>20</td>
<td>0,2</td>
<td>225</td>
<td>22,9</td>
</tr>
<tr>
<td>100</td>
<td>40</td>
<td>0,4</td>
<td>200</td>
<td>31,4</td>
</tr>
<tr>
<td>$\varepsilon_{\text{IL}}=20$</td>
<td>$\varepsilon_{\text{IL}}=80$</td>
<td>$\varepsilon_{\text{IL}}=120$</td>
<td>$\varepsilon_{\text{IL}}=20$</td>
<td>$\varepsilon_{\text{IL}}=80$</td>
</tr>
</tbody>
</table>

Figure 42: Calculated thickness of a assumed interfacial layer. An almost linear behavior is obtained for various Pt/Ti bottom electrode thicknesses and for different values of the dielectric constant of the assumed interfacial layer.

In the literature formation of an interfacial TiOx layer by diffusion of Ti through the platinum bottom electrode is discussed [Bru91]. However, no diffusion of Ti on top of bottom Pt is seen (see e.g. AES in Figure 21b). Therefore, the formation of a interfacial TiOx layer seem not to be very likely the root cause for the lower polarization values by using Pt/Ti electrodes versus Pt/TiOx electrodes although a TiOx layer with a dielectric constant of 80 could explain the lower values of the polarization and dielectric constant of the total film (the possible chemical nature of the interfacial layer will be discussed below).
Since neither an interfacial TiOx layer nor incorporation of Ti inside the SBT are considered as the root causes for the lower polarization values seen on Pt/Ti electrodes another mechanism has to be responsible. It is reported [Koi97] that excess of bismuth is necessary for SBT of excellent quality. Content of bismuth in SBT during anneal is crucial for the crystallization process. Therefore, the lower content of Bi inside SBT layer due to the enhanced diffusion of bismuth to the Pt/Ti bottom electrode has to be considered for the lower polarization values.

From the content of Bi in the Pt/Ti bottom electrode ([Bi]=2.37µg/cm²) and the content of Ti in the bottom electrode ([Ti]=4.51µg/cm²), the percentage of the titanium which had reacted with Bi to form BiTi₃O₉ (BTO) can be calculated. For stochiometric BTO (Bi₄Ti₃O₁²) the maximum ratio of Ti reacted with Bi is

\[
\frac{Bi/Ti \, exp.}{Bi/Ti \, theory} = \frac{[Bi]/[Ti]}{(4 \cdot M_B)/(3 \cdot M_T)} = \frac{2.37/4.51}{(4 \cdot 208.98)/(3 \cdot 47.87)} = 0.09
\]

Therefore, a maximum ratio of 9% of the titanium in the bottom electrode can have reacted to stochiometric BTO. Allowing a non-stochiometric reaction of Bi and Ti by ignoring the 4 and 3 in eq. 26, the composition of the resulting compound is BiTi₃.₆O₉.

Also, enhanced diffusion of Bi to the Pt/Ti electrode will leave a Bi deficient layer next to the Pt bottom electrode. As a result an interfacial layer like SrTaₓOᵧ can be formed. By assuming a dielectric constant of 120 for SrO-Ta₂O₅ [Lan59], the thickness of this layer can be calculated. For the Pt(100nm)/Ti(10nm) bottom electrode, the thickness of the assumed interfacial SrTaₓOᵧ layer with ε=120 is 15nm (Figure 42). Therefore, it is very likely that the formation of a Bi deficient interfacial layer between the bottom electrode and the SBT film has to be considered for the lower polarization values seen on Pt/Ti electrodes.

As shown above (Figure 36), higher polarization values are obtained for Pt bottom electrode sputtered at 550°C. Sputtering the Pt at 300°C or RT did not alter the electrical properties. Sputtering the Pt at higher temperatures results in a denser Pt film compared to a Pt film sputtered at RT. Comparing the AES profiles of SBT/Pt/Ti films after SBT crystallization with Pt sputtered at 300°C and at RT, more diffusion of Ti inside the Pt layer is seen for the Pt layer sputtered at RT [Nas98]. Therefore, higher polarization values are expected for Pt deposited at higher temperatures if reduced Bi loss into Pt electrodes with reduced Ti content is assumed.

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6 Average of 2.59, 2.29 and 2.23µg/cm² of the Bi content after SBT etch on Pt/Ti electrodes (see Figure 41)

7 The density of Ti is 4507 kg/m³ or for a 10nm Ti film 4.507µg/cm² (see Figure 10 on page 19)
Summary

Titanium was always diffusing into platinum when using Pt/Ti bottom electrode. The higher the ratio of Ti/Pt thickness used the lower the polarization values and the higher the coercive voltages on Pt/Ti electrodes. Using Pt/TiO$_x$ electrodes no diffusion of Ti inside Pt was found and the highest polarization values were measured for this electrode. Therefore, indirect poisoning of SBT with Ti was assumed to be responsible for the degradation of the electrical properties by using Pt/Ti electrodes. However, as showed by direct poisoning of SBT with Ti (Ti doping of SBT or sputtering of interfacial Ti layer), low polarization values are only seen, if high amount of Ti doping and a thick Ti interfacial layer were used. But no Ti was found inside SBT by using standard Pt/Ti electrodes as shown by AES. Therefore, neither an interfacial TiO$_x$ layer nor incorporation of Ti inside the SBT are considered as the root causes for the lower polarization values seen on Pt/Ti electrodes. Another mechanism has to be responsible. It was shown, that the loss of bismuth into the Pt/Ti was higher than the loss of bismuth into the Pt/TiO$_x$ electrode. For the Pt/Ti electrode 4.7% of the bismuth is lost into the Pt/Ti electrode. It was calculated that a maximum ratio of 9% of the titanium in the bottom electrode can have reacted with the Bi to stochiometric BTO. It is now assumed that this loss of bismuth is causing the lower polarization values for the Pt/Ti electrode. Firstly, crystallization process is impaired by the loss of bismuth and secondly the formation of a Bi deficient interfacial layer with a lower dielectric constant of about 120 will result in lower polarization values.

The dielectric constant of this interfacial layer could be determined more accurately by producing a series of Pt/SBT/Pt/Ti capacitors with different thickness. Plotting 1/C versus film thickness should help revealing the dielectric constant of the interfacial layer. Also, if there is no or a significant thinner interfacial layer present on Pt/TiO$_x$ electrodes compared to Pt/Ti electrodes, which will allow to reduce film thickness much further without any loss of polarization as indicated in Figure 38, still needs to be proven for films <<100nm.
5. SBT layer processing

5.1. Introduction

Among many deposition techniques like sputtering methods (PVD), metal-organic vapor deposition (MOCVD) [Hin98] [Iso97] [Li96] [Ish99], Liquid Source Misted Chemical Deposition (LSMCD) [Sol98] [McM94] [Hay94] [Koi98b] [McM92] and pulsed laser deposition (PLD) [Pig00b] [Ras99], Metal Organic Decomposition (MOD) is used because it is simple, cheap, homogeneous in film thickness ($3\sigma<5\%$ with $\sigma$ being the standard deviation), fast to process and easy to modify (e.g. stochiometry). Details about SBT MOD processing like type of solution, diluting, description of spin coating process, layer sequences and standard thermal treatments are given in chapter 3.1 on page 27 or elsewhere [Sco96] [Ara96] [Tri99] [Ahl99].

![Figure 43: (a) SEM cross-section pictures of patterned Pt/IrOx/Ir bottom electrode stack with SBT and top electrode. (b) Optical microscopy picture of patterned Pt/IrOx/Ir bottom electrode (height 350nm) after SBT coating and crystallization anneal. Data shown are values for SBT thickness.](image)

Bottom electrode topography and SBT thickness

By using a patterned non-planar bottom electrode (which is the case for a true 3D integration concept, see Figure 13a) several issues arise with the MOD technique. Due to the planarization effect of spin coating a planarization factor ($d_{SBT}$ thickness of SBT layer on top of desired feature / $d_{SBT}$ thickness of layer on un-patterned area) of e.g. 0.5 is obtained (see Figure 43a). A factor of 1 means no planarization effect at all. This factor depends on the MOD process used and on the structures being looked at (Figure 43b).
Therefore, the thickness of the ferroelectrics depend on (i) the vertical dimension or height (Figure 44a) and (ii) on the lateral dimension or area (Figure 44b) of the storage node. The thicker and the smaller the patterned bottom electrode or storage node, the thinner the film thickness of the ferroelectric layer.

Figure 44: (a) SBT film thickness as measured by reflectometer in the center of a 1mm² (1⋅10⁶µm²) patterned bottom electrode. Two SBT layers were used and the different thickness of the bottom electrode was achieved by using Pt/Ti or Pt/IrOₓ/Ir combinations with Pt being always the top layer. (b) SBT thickness versus area for a single SBT layer. SBT thickness on the 1⋅10⁶µm² area was measured with the reflectometer and with the SEM on all smaller areas. For the 1⋅10⁶µm² and the 1⋅10⁶µm² area the lateral dimension of the squares was 1µm and 1000µm respectively. For the 4⋅10³µm² area, different capacitors in the shape of fingers with a min. lateral feature size of 1, 4 and 32 µm were used. Also shown in b) is a schematic drawing of the orientation of the finger structures on the wafer as seen for the SBT spin-on process.

SBT thickness is not only studied on squares but also on finger shaped electrodes. The lateral dimensions of the fingers are 1, 4, and 32µm although the total area is always 4⋅10³µm² (see inset in Figure 44b for illustration of the finger structure as well as for the orientation of the fingers). In Figure 44b the SBT thickness is plotted for 1⋅10⁶µm² storage node (lateral dimension 1µm), 4⋅10³µm² finger electrodes (lateral dimension 1,4,32µm with 64, 16 and 2 fingers respectively) and for 1⋅10⁶µm² large capacitors (lateral dimension 1000µm). As can be seen in Figure 44b a clear difference between the SBT thickness on the 1⋅10⁶µm² storage node (1µm) and the smallest 4⋅10³µm² fingers (1µm) is observed although the lateral dimension is 1µm for both structures. This result shows that the SBT thickness by spin-on coating is

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8 To overcome this non-uniform thickness problem, only thin Pt/Ti bottom electrodes were used and only Pt2 capacitors were measured with the Pt1 bottom electrode being larger than the smaller patterned Pt2 top electrode and SBT layer. For this capacitor the SBT thickness can be assumed to be uniform.
mostly determined by the area and not by the lateral dimension of the electrode. Due to the catalytic effect of Pt for instance or other loading effects, this result may also be true for other deposition techniques.

**Crystallization anneals**

The most important process step in ferroelectric layer processing is the crystallization anneal. Investigation of the annealing conditions of SrBi$_2$Ta$_2$O$_9$ (SBT) films showed that crystallization behavior and grain growth and therefore polarization values are significantly affected by RTP process (chapter 5.2.1) and crystallization anneal. Besides the standard crystallization anneal in oxygen (chapter 5.2.2), the anneal in nitrogen (chapter 5.2.4) or under low pressure (chapter 5.2.3) are also studied.

**Theoretical prediction of the limitation of crystallization anneal temperature for SBT based on AFM results**

Large SBT grains usually give high polarization values. However, large grains are generally undesirable due to variations of the cell-to-cell reproducibility when the grain and feature size approaches each other. On the other hand, fine-grained Perovskite oxides are favored due to their lower electrical conductivity and higher breakdown voltages caused by the formation of inter-grain depletion layers [Sco98].

![AFM Image, z-range [nm]](image)

**Figure 45:** Z-range of AFM images for 5×5µm$^2$ scans of SBT/Pt/Ti samples annealed at different temperatures. The SBT films thickness was 180nm. Each data point is the average of 6 measurements. The data shown are taken from Figure 47. The influence of the Pt bottom electrode roughness can be neglected.

![Capacitor screen yield versus capacitor area [µm$^2$]](image)

**Figure 46:** Capacitor screen yield versus capacitor area for different lots. Samples were processed with 800°C, 725°C and 700°C crystallization anneal. SBT films thickness was 180nm. For the 800°C samples shorted capacitors are measured in the area range shown, whereas no shorts are measured for the 700°C and 725°C annealed samples.
Generally, SBT thin films deposited on Pt(111) electrodes should always show (00L) preferential orientation or polycrystalline structure due to the lattice match [Hu99]. SBT tends to grow in the (115) orientation (see e.g. Figure 76 or [Fuj98]). The (115) direction is connected with an elliptical grain growth also called rod-like structure (see e.g. Figure 15d on page 27). The rod-like morphology is connected with a large degree of porosity, due to the difficulty connected with close packing of elliptic grains. Due to this porosity, the shorting behavior of SBT capacitors becomes a function of the SBT thickness and the annealing temperature. For instance, SBT films with thickness <120nm annealed at 800°C give only shorted capacitors. Therefore, to achieve ultra thin SBT films, a low temperature process is needed [Moe02].

Figure 47: Z-range of AFM image with different scan sizes or area of SBT samples annealed at different temperatures. The SBT films thickness was 180nm. Each data point is the average of 3-14 measurements. See text for more details.

Figure 48: Extrapolated area out of Figure 47 at which shorts should be measured. Assuming a capacitor area of $6.04 \times 10^6 \mu m^2$ (4Mb $1.2 \mu m \times 1.2 \mu m = 4.2^{20} \times 1.44 \mu m^2$) only crystallization temperatures equal or below 675°C will be sufficient.

In Figure 45 the z-ranges of AFM images taken from SBT surfaces are plotted versus annealing temperature. As can be seen in Figure 45, SBT crystallization starts at around 650°C. Below 650°C, the z-range of the AFM image does not change with temperature whereas at 650°C and above the z-range increases linearly. This is due to increased grain growth at elevated temperatures. Therefore, voids, porosity and the z-range of the AFM images increase also with temperature. In consequence, after deposition of top electrode and capacitor formation, the probability to find a shorted capacitor is also increasing with annealing temperature and capacitor area (Figure 46). For the 800°C crystallization...
anneal, shorted capacitors are measured starting from 100µm². From 100000µm² up all capacitors are shorted. No shorts were measured for 700°C and 725°C annealed samples.

In Figure 47 the z-ranges of AFM images with different scan sizes taken from SBT samples annealed at different temperatures are shown. The lines shown are best-fit results. As shown in Figure 46, for 800°C annealed samples shorted capacitors are measured starting from 100µm and from 1×10⁵ µm² on all capacitors are shorted. This area range (dotted lines in Figure 47) corresponds to 100nm up to 130nm in z-range of the AFM scan (bold line in Figure 47). Assuming identical behavior for all other samples annealed at different temperatures with the same thickness, the smallest area at which a short should be measured can be extrapolated. Therefore, shorted capacitors should be measured starting from 2×10⁵ µm² for 700°C, from 3×10⁶ µm² for 675°C sample and from 4×10¹¹ µm² for 650°C annealed sample. For the samples without crystallization anneal (sample “no FeA”) [Har00f], shorts are not relevant at all. Extrapolated areas at which shorts should be measured out of Figure 47 versus temperature are shown in Figure 48. Assuming a capacitor area of 6.04×10⁶ µm² (4Mb·1.2µm·1.2µm = 4·2²·1.44µm²) only crystallization anneal temperatures below 675°C will be sufficient for a short-free capacitor cell array. Therefore, the demand for a low temperature process is not only driven by the integration aspects of the poly-Si plug and the O₂ barrier system, but also by the reliability concerns of integrated capacitors.

5.2. Crystallization anneal

5.2.1. Rapid Thermal Processing for Crystallization of SBT Thin Films

SBT films have to go through a cycle of solution deposition, baking, and annealing as described in the chapter 3.1 on page 27. Optimized processes for SBT films using annealing process modifications are studied. The use of Rapid Thermal Processing (RTP) in various semiconductor processes has been on the rise for the past several years. Therefore, the influence of RTP on crystallization behavior and electrical properties is investigated. Also, the possibility of substituting the diffusion anneal by a rapid thermal crystallization anneal in order to reduce thermal budget and exposure to O₂ at high temperature is studied [Jos98]. The different annealing sequences as listed in Table 3 are used.

The x-ray diffraction spectra look very similar for the films that were furnace annealed (e.g. samples 1-3). The film with no furnace anneal (only RTP at 800 °C, sample 4) shows XRD peaks of relatively low intensity and slight broadening at the base indicating smaller grains. In Figure 49 the SEM cross-sections of SBT film samples on Ti/Pt electrodes are shown. The films (samples 1 and 2), which were subjected to RTP and furnace, anneal resulted in larger grain size (100-150nm) whereas the films (samples 3 and 4), which were subjected to only RTP or furnace anneal show smaller grains (75-100nm). The cross-sectional SEM micrographs show dense film structure for film 1 and 2, which experienced a two-step anneal
process (RTP + diffusion furnace) while samples 3 and 4 show some porosity, especially at the interface of two SBT layers. Even a furnace anneal for 60min. was not enough to eliminate this porosity (sample 3).

Table 3: RTP and furnace anneal process modifications for different samples. SBT film thickness was 180nm (double layer) for samples 1-4 and 90nm (single layer) for samples A-C.

Figure 49: Cross-sectional SEM micrographs of SBT films on Ti/Pt electrodes with different annealing processes. (a) sample 1, (b) sample 2, (c) sample 1, and (d) sample 4. Smaller grain size and trapped porosity between the two
SBT layers can be seen in samples 3 and 4. SBT layers in samples 1 and 2 (two-step anneal) are relatively denser. The dark spots at the Pt underlayer are due to diffusion and oxidation of Ti during the annealing process.

The SBT surfaces of samples processed almost identically to samples 1 and 3 except the temperatures for RTP and crystallization anneal were set to 650°C and 725°C respectively, are shown in Figure 50. Only for the two-step anneal methodology with RTP process and crystallization anneal (Figure 50a), a dense film with large grains and clusters are observed. Without the RTP process (Figure 50b) grains are smaller.

![Figure 50: SEM micrographs of SBT surfaces processed similar to sample 1 and 3 except RTP temperature was 650°C and the crystallization temperature 725°C. (a) after RTP and crystallization anneal (similar as sample 1), (b) after crystallization anneal only without RTP process step (similar as sample 3).](image)

Figure 51: Effect of RTP on grain structure of SBT. SEM pictures of group A samples with variation of the RTP temperature (a) 575°C and (b) 750°C. SBT film thickness was 90nm (single layer films) and ferro anneal for all samples was 725°C.
Figure 52: Effect of RTP of group A samples with variation of the RTP temperature from 575°C up to 750°C. (a) SBT film thickness and index of refraction, and (b) hysteresis loops. SBT film thickness was 90nm (single layer films) and ferro anneal for all samples was 725°C.

Figure 53: Effect of RTP on grain structure of SBT. SEM pictures of group C samples with variation of the RTP ramp rate from 10°C/s up to 50°C/s. SBT film thickness was 90nm (single layer films) and ferro anneal for all samples was 725°C.

The I-V characteristics of the films are quite similar with leakage current densities on the order of $10^9$ A/cm² at 3V. At higher voltages, the film with no furnace anneal (sample 4) shows minimum leakage which can be attributed to lower porosity and smaller grains (see Figure 45 and [Jos98]). As seen from the hysteresis loops, SBT films which were exposed to a two step anneal (RTP + furnace anneal) have larger switched charge (20%) compared to the films subjected to either RTP or diffusion (furnace) anneal [Jos98]. The films were stressed and tested at 85°C with 3V amplitude for measuring the imprint characteristics ($10^9$ negative unipolar pulse train before measuring the switched and unswitched charge). It
is found that the film with two-step anneal, one RTP followed by diffusion anneal (sample 2) shows maximum resistance to imprint [Jos98].

In Figure 51 the SBT surface of group A samples after RTP process with different temperatures (575°C, 750°C) plus crystallization anneal (725°C) are shown. In Figure 52 SBT film thickness, index of refraction and hysteresis loops after RTP process (575°C-750°C) plus crystallization anneal (725°C) are shown. The higher the RTP temperature the denser the film with SBT clusters, the higher the refraction index and the higher the polarization values get. No or only little influence is seen for the variation of the RTP time (group B samples).

In Figure 53 the SBT surface of group C samples after RTP process with different ramp rates (10°C/s, 25°C/s, 50°C/s) plus crystallization anneal (725°C) are shown, and in Figure 54 results of SBT film thickness, index of refraction and hysteresis loops of these samples are presented. The higher the ramp rate of the RTP process the denser the film with SBT clusters, the higher the refraction index and the higher the polarization value gets. No difference of composition of SBT surfaces between samples with 10°C/s and 50°C/s ramp rate is seen by AES.

![Figure 54: Effect of RTP of group C samples with variation of the RTP ramp rate from 10°C/s up to 50°C/s. (a) SBT film thickness and index of refraction, and (b) hysteresis loops. SBT film thickness was 90nm (single layer films) and ferro anneal for all samples was 725°C.](image)

5.2.2. Crystallization anneals in oxygen ambient

In Figure 55 the effect of the crystallization or ferro anneal after performing the RTP process is shown for 50nm and 90nm single SBT layer, and 180nm double layer SBT films. For the 650°C annealed samples, single SBT grains are embedded in an amorphous matrix (Figure 55a, left column). The number of grains increases for the 90nm SBT film annealed at 650°C compared to a 50nm SBT film.
<table>
<thead>
<tr>
<th>Layer Type</th>
<th>Temperature</th>
<th>SEM Pictures</th>
</tr>
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<td>a) 650°C</td>
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<tr>
<td></td>
<td>b) 700°C</td>
<td>![SEM Picture]</td>
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<td></td>
<td>c) 800°C</td>
<td>![SEM Picture]</td>
</tr>
<tr>
<td>90nm single layer</td>
<td>a) 650°C</td>
<td>![SEM Picture]</td>
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<tr>
<td></td>
<td>b) 700°C</td>
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<tr>
<td></td>
<td>c) 800°C</td>
<td>![SEM Picture]</td>
</tr>
<tr>
<td>180nm double layer</td>
<td>a) 650°C</td>
<td>![SEM Picture]</td>
</tr>
<tr>
<td></td>
<td>b) 700°C</td>
<td>![SEM Picture]</td>
</tr>
<tr>
<td></td>
<td>c) 800°C</td>
<td>![SEM Picture]</td>
</tr>
</tbody>
</table>

Figure 55: Effect of ferro anneal and number of layers on grain structure of SBT. SEM pictures of samples with (a) 650°C, (b) 700°C and (c) 800°C ferro anneal are shown.

<table>
<thead>
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<th>Layer Type</th>
<th>Temperature</th>
<th>SEM Pictures</th>
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<td>![SEM Cross Section]</td>
</tr>
<tr>
<td></td>
<td>b) 700°C</td>
<td>![SEM Cross Section]</td>
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</table>

Figure 56: SEM cross section pictures of samples with 700°C ferro anneal with (a) single SBT layer and (b) with double SBT layers are shown.
Single-layered films annealed at 700°C are smooth (see x-section in Figure 56a) and exhibit secondary phases (Figure 55b, top picture). Double-layered films are rough (see x-section in Figure 56b) and no secondary phases are seen (Figure 55b, bottom picture). Grain size and morphology of SBT films annealed at 800°C are almost independent of thickness (Figure 55c, right column). For all the films annealed at 800°C fully crystallized SBT grains are observed.

Figure 57: (a) Refractive index for single-layered SBT films (thickness <90nm) versus film thickness. (b) SBT film thickness and index of refraction for double-layered SBT films versus crystallization anneal temperature (RTP step before crystallization anneal was performed at 650°C).

Figure 58: (a) Effect of ferro anneal temperature. Hysteresis loops after different crystallization anneals for 90nm single layer SBT films (no RTP step was performed). (b) Effect of the ferro anneal time from 0 up to 13h. Shown are polarization values versus ferro anneal time for nitrogen process (ONNN) on Pt/Ti electrodes and for oxygen
process (OOOO) on Pt/Ti and Pt/TiOx electrodes. Details about ONNN and OOOO process are given in the next chapter 0. "No FeA" means no ferro anneal at all and only the RTP is performed and "push/pull" means that the quartz boat with the wafers is moved into the furnace and then removed immediately after reaching the center of the furnace. The travelling time of the boat for “push and pull” was 10min each.

It is noticed that the higher the crystallization temperature gets the higher are the measured polarization values (Figure 58a). Due to SBT crystallization, SBT film thickness is decreasing and index of refraction is increasing (Figure 57b), if the crystallization anneal temperature exceeds the process temperature of the RTP. For single layer films with thickness <90nm refractive index is increasing (Figure 57a) and polarization values are decreasing due to the formation of secondary phases like the fluorite structure (see chapter 2.3 on page 16).

As in the chapter above about RTP processing, ramp rate was also studied for the furnace anneal. However, no or only very little influence is seen. The effect of the crystallization anneal time is shown in Figure 58b. Due to diffusion and grain growth, polarization values are increasing with time.

5.2.3. Low pressure crystallization anneals

In order to reduce or to avoid oxidation of the poly-silicon plug underneath the bottom electrode stack, crystallization anneals at low pressure are studied [Tri99]. The process flow is identical to the standard process used throughout this entire work (see chapter 3.1 on page 27) except that the crystallization anneal is performed at low pressure. In Figure 59 the effect of low pressure crystallization at <0.1mbar, 1.3mbar, 13mbar and 80mbar on the hysteresis loops is shown. The temperature for the crystallization anneal was 725°C for all samples. For reference the hysteresis loop annealed at atmospheric pressure is also shown. The temperature of the post anneal after capacitor formation was 725°C at atmospheric pressure for all samples. Highest 2P_r polarization values of 18-19µC/cm² are seen for the low-pressure crystallization anneals at 1.3mbar and 13mbar and lowest values are seen for the low pressure anneals at <0.1mbar. For the standard anneal at atmospheric pressure 16µC/cm² are obtained. Leakage currents are also lowest for samples annealed at 1.3mbar and 13mbar whereas values for the coercive field are the same for all samples.

In Figure 60 the SEM pictures of SBT surfaces annealed at <0.1mbar, 13mbar and 80mbar are shown. The SBT film annealed at <0.1mbar consists of small grains embedded in a secondary phase. The sample annealed at 13mbar show the largest cluster formation, whereas at 80mbar the cluster formation and grains

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<0.1mbar means the lowest pressure possible with the existing rotary pumping system without any gas flowing. For the other pressures, chamber pressure was adjusted with a butterfly valve at flowing oxygen. 1Torr=1.333mbar.
sizes are slightly reduced. AES curves of Pt/Ti/SiO2 samples annealed at 700°C at <0.1mbar and 13mbar are shown in Figure 61. The sample annealed at 13mbar show the typical Ti(Ox) curves already seen in e.g. Figure 21b on page 42 in chapter 4.2.1. Ti is oxidized before diffusing up to the surface. This indicates that during the 13mbar anneal sufficient oxygen is flowing to cause typical Ti oxidation. However, the AES curves of the <0.1mbar anneal look different. This time Ti is even found on the Pt surface. Therefore, oxygen content during annealing at <0.1mbar is not sufficient to cause oxidation of titanium and to prevent Ti diffusion up to the surface.

Figure 59: Effect of low pressure crystallization anneal at <0.1, 1.3, 13, 80mbar and at atmospheric pressure on hysteresis loops. Crystallization anneal temperature was 725°C and SBT film thickness was 90nm (single layer). Top electrode deposition was done by DC sputtering and patterning by RIE etch with conventional photo resist.

a) <0.1mbar  

b) 13mbar  

c) 80mbar

Figure 60: SEM pictures of SBT surfaces after crystallization anneal at different pressures. (a) <0.1mbar, (b) 13mbar and (c) 80mbar.
5.2.4. Crystallization anneals in nitrogen ambience

To protect the poly-silicon plug underneath the bottom electrode stack from oxidation at elevated annealing temperatures, crystallization anneals in nitrogen are studied. The process flow is identical to the...
standard MOD process described in chapter 3.1 on page 27 except that the crystallization anneal is performed in nitrogen (Figure 62). Using for the four anneals “pre-anneal, RTP process, ferro anneal and post anneal” the capitals “O” or “N” for oxygen or nitrogen anneal, the following short forms for the standard process in oxygen and nitrogen are obtained: OOOO and ONNN.

AES curves of samples with –NNN, NNNN, OOOO and ONNN process are shown in Figure 63. After SBT processing in nitrogen without bottom electrode anneal (Figure 63a) or performing the bottom electrode anneal in N₂ (Figure 63b) according to the –NNN or NNNN process respectively, interdiffusion of Ti inside the SBT layer is seen. Electrical results of these samples are very poor. However, samples
with SBT processing in nitrogen and with pre anneal in O\textsubscript{2} (ONNN, Figure 63d) shows identical AES profile as OOOO process (Figure 63c). No interdiffusion of Ti inside SBT is seen for these two processes. Therefore, the favored process for the nitrogen process is the pre anneal in oxygen.

![Figure 64: RTP process step used for N\textsubscript{2} processes.](image)

![Figure 65: (a) 2P\textsubscript{r} values for the ONxN process with increasing N\textsubscript{2} to O\textsubscript{2} content in the ferro anneal. (b) 2P\textsubscript{r} Polarization values of the Oxxx processes with the pre anneal in O\textsubscript{2} (x means RTP, ferro anneal and post anneal are either in O\textsubscript{2} or in N\textsubscript{2}). The temperature of the ferro and post anneal was 800°C.](image)

In Figure 64 the modified RTP process step for the nitrogen process is shown. Before ramping to the high temperature, a low temperature step in O\textsubscript{2} (A) at 400°C is inserted to burn off the remaining organic. Without the low temperature step in O\textsubscript{2}, wafers turn hazy if the entire annealing process is performed in
N₂ only. After a steady state for the low temperature step in O₂ for about 60s, the chamber is flushed with N₂. With the chamber being oxygen-free the wafers can be ramped to the high temperature (B).

Figure 66: 
Fatigue values for the Oxxx processes.

Figure 67: SEM pictures of the SBT surfaces for the OOOO and the ONNN process after coating and RTP process, and after ferro anneal at 800°C.
In Figure 65a 2P values for the ONxN process with increasing N\textsubscript{2} to O\textsubscript{2} content in the ferro anneal are shown. With a ratio of the N\textsubscript{2} to O\textsubscript{2} content of above 0.9, the polarization values increase by 21%. In Figure 65b all O and N anneal combinations for Oxxx process are shown. Oxxx means the pre anneal is performed in O\textsubscript{2}, and RTP, ferro anneal and post anneal are either done in O\textsubscript{2} or N\textsubscript{2}. It is clearly seen that the more N\textsubscript{2} anneals are used the higher the polarization values get. However, doing the post anneal in N\textsubscript{2} (OxxN) leads always to slightly lower polarization values (Figure 65b) and higher fatigue (Figure 66) compared to the samples with the post anneal in O\textsubscript{2} (OxxO). The temperature of the ferro and post anneal was always 800°C.

In Figure 67 SEM pictures of the SBT surfaces for the OOOO and the ONNN process after coating and RTP process, and after ferro anneal at 800°C are shown. After coating and the two-step N\textsubscript{2} RTP process already small grains are seen for the SBT ON\textsuperscript{3} process. After crystallization or ferro anneal at 800°C rod like SBT grains are obtained for the O\textsuperscript{4} process whereas for the ON\textsuperscript{3} process more circular grains are seen.

**5.2.5. Discussion**

SBT layer processing with RTP process step before crystallization anneal is found very crucial. RTP process initiates and forms nucleation sites. Since SBT films without RTP processing show smaller grains, no cluster formation, presence of porosity and lower polarization values, many nucleation sites from defects in the SBT layer or from the interface to the bottom electrode will act as seeds spots for the grain growth during subsequent high temperature diffusion anneal. The many nucleation sites and therefore the many grains are not able to form a dense SBT layer with large cluster formations. If a RTP process step is performed before the high temperature diffusion anneal, larger SBT gains, SBT clusters, higher refraction index and higher polarization values are obtained. It is also found that the higher the temperature of the RTP process and the higher the ramp rate, the larger the SBT gains and clusters, and the higher the polarization values get. Time for the RTP process does not influence any of these results. This means during the fast ramp up of the RTP process step only a few nucleation sites are being formed whereas during the slow ramp up in a furnace (without the RTP process before) many nucleation sites are being formed. The fewer seeds spots after RTP process promote a denser grain growth.

Bi content on the SBT surface after RTP processing was checked by AES. No difference in Bi composition or Bi evaporation for the samples with e.g. 10°C/s and 50°C/s RTP process was found. Therefore, Bi seems not to cause the different crystallization behavior but the difference in the formation of the nucleation sites as discussed above.

The high temperature crystallization diffusion anneal after RTP process leads to grain growth. The effects of crystallization anneal temperature and SBT film thicknesses are summarized in Figure 68. The SBT
phase crystallizes between 625-650°C. If the temperature of the ferro anneal exceeds the RTP temperature (typically 650°C), SBT film thickness is decreasing and refractive index is increasing due to crystallization of SBT. The higher the crystallization temperature the larger the SBT grains and the higher the polarization values. For SBT films <90nm annealed between 650°C and 700°C, SBT grains are embedded in an amorphous matrix or show secondary phases which result in an increase of refractive indexes. The secondary phase is most likely the fluorite phase since this phase disappears at higher annealing temperatures whereas for instance the pyrochlore phase does not. For thicker films while using the same RTP process and keeping the crystallization temperature below 700°C, more SBT grains are embedded in an amorphous matrix. Therefore, the thicker the SBT film the more nucleation sites and grains can be formed, the rougher the film and the less secondary phases are left. At 800°C crystallization anneal SBT grains are largest and its structure is almost independent of the film thickness since the temperature is well above the initial crystallization temperature. The large grains with voids at higher crystallization temperatures are responsible for shorts in SBT films <120nm.

![Figure 68: Effect of crystallization anneal temperature and film thickness on grain size, refractive index n and polarization for SBT.](image)

To reduce the chance of oxidation of the poly- silicon plug underneath the bottom electrode, low pressure crystallization anneal are studied. The vapor pressure can be expressed as [Gme64]

$$\log p = \frac{A}{T} + B \log T + C$$  \[eq. 27\]

with $p$ being the vapor pressure and $T$ the temperature in Kelvin. Using the constants $A=10400K$, $B=-1.26$, and $C=12.35$ for elemental bismuth, the vapor pressure of Bi becomes 14.1mbar at 725°C or
998°K. Lowest polarization values are measured for crystallization anneals at <0.1mbar. This pressure is well below the vapor pressure of the Bi. Therefore, the SBT films get highly Bi deficient leading to incomplete crystallization, small grains, formation of secondary phases and therefore to low polarization values [Koi97]. The formation of an interfacial layer due to Ti diffusion up to the SBT layer can be neglected since a bottom electrode anneal at atmospheric pressure in O_2 is usually performed before SBT coating and low pressure annealing. During this anneal Ti is oxidized to prevent Ti diffusion up to the surface (see chapter 4.2.1 on page 40). However, the result of the low pressure bottom electrode experiment (see Figure 61a) shows that oxygen supply during anneal at pressures <0.1mbar is not sufficient. Therefore, evaporation of Bi and low oxygen supply at crystallization anneals <0.1mbar cause degradation of the ferroelectric properties. Highest polarization values, lowest leakage currents and dense grain structures are obtained for crystallization anneals at 1.3 or 13mbar with flowing oxygen whereas slightly lower polarization values are obtained for crystallization anneals at 80mbar or at atmospheric pressure. The increase in polarization after low-pressure crystallization at 1.3mbar or 13mbar is assumed to be due to some depletion of metallic bismuth usually left over at the grain boundaries after crystallization. At crystallization anneals well above the vapor pressure of Bi, metallic Bi left over at the grain boundaries may pin the domain walls, which will result in lower polarization values [Kim99]. Therefore, the best pressure range for the 725°C crystallization anneal is between 1.3mbar and 13mbar, whereas for the 650°C crystallization anneal the optimum pressure range was 3mbar (vapor pressure 2mbar) [Oga98].

Two out of the four anneals in a typical capacitor module process flow (bottom electrode or pre anneal, RTP, crystallization or ferro anneal, and post or recovery anneal) are found to be replaceable by anneals in nitrogen. Performing the pre anneal or electrode anneal in nitrogen, leads to diffusion of titanium up to the platinum surface. After pre annealing the electrode in nitrogen, the titanium is poisoning the ferroelectric layer after deposition of SBT. Therefore the preferred electrode anneal is performed in oxygen. After SBT coating, hazy films are obtained if RTP process step is done in pure nitrogen. Remaining organic material of the metal organic components in the film is reacting at elevated temperatures. However, it is possible to burn off the organics at lower temperatures in oxygen followed by a high temperature step in nitrogen. Afterwards, no degradation of the film is seen. Also, grains become already larger with the two-step oxygen/nitrogen RTP process compared to the pure oxygen process. A crystallization anneal in nitrogen does not alter the ferroelectric properties either. There is even an increase of polarization seen after crystallization anneal in nitrogen. This can again be attributed to the evaporation of some metallic bismuth
as discussed above due to the low partial pressure of oxygen during the nitrogen anneal\textsuperscript{10}. However, post anneal in nitrogen after capacitor formation leads to slightly lower polarization values, higher leakage current and higher fatigue characteristics. Post anneal in oxygen seem to be necessary to recovery the damages after patterning. Nitrogen leaves oxygen vacancies, which act as charge trapping sites leading to pinning of domains. Therefore, post anneal in nitrogen results in accelerated fatigue characteristics. Therefore, the best process sequence with nitrogen anneals becomes ONNO with the pre anneal in O\textsubscript{2}, RTP and crystallization anneal in N\textsubscript{2} and the post anneal in O\textsubscript{2}.

To conclude. RTP process is found crucial to promote nucleation and grain growth. RTP or crystallization anneal operated close to the vapor pressure of Bi (low pressure or nitrogen anneal) improves ferroelectric characteristics\textsuperscript{11}.

\textsuperscript{10} Performing the crystallization anneal in a closed RTP chamber with nitrogen flowing results as for the <0.1mbar low pressure furnace anneal also in degraded ferroelectric properties since O\textsubscript{2} partial pressure is too low.

\textsuperscript{11} Unfortunately, bottom electrode stacks with a IrO\textsubscript{x} oxygen barrier cannot withstand nitrogen or low pressure anneals since IrO\textsubscript{x} de-oxidizes very easily [Pin01]. Therefore, nitrogen or low pressure anneals are not compatible with the integration schemes for stack cells (see e.g. Figure 13).
6. Capacitor formation, patterning and recovery anneal

6.1. Introduction

For the formation of the ferroelectric capacitor, the Pt top electrode, the ferroelectric layer and the bottom electrode have to be structured. Pt top electrodes, which are deposited on the ferroelectric layer through a shadow mask without etching the platinum, is frequently used. Using this technique it has been found that no recovery anneal is necessary to achieve good leakage performance. This is possible by adjusting stoichiometry, crystallization anneal temperature [Nog96] and the RTP process [Wat97]. However, integration of ferroelectric thin films for high-density memory applications requires the etching of Pt/SBT/Pt stack for capacitor formation. This is evident for the offset cell structure [Moa95] where either the bottom or top electrode of the structured capacitor is connected via a metal strap to the underlaying transistor (see e.g. Figure 11 on page 24). Patterning of the top electrode and ferroelectric layer is also necessary for the stacked capacitor cell where the storage node is not formed by the top electrode but by the bottom electrode which is connected via a plug to the transistor underneath (see e.g. Figure 12 on page 24). In this case each cell has to be patterned to open the contact hole for the bit line. Further, for all other integration concepts shown in chapter 2.5 (page 23), patterning of the Pt/SBT/Pt stack by RIE is necessary.

Since noble metals and ferroelectric materials are hard to etch by conventional etch processes, sidewall depositions and tapered sidewalls for the capacitors are obtained [Del99] [Kwo00] [Eng99] [Yun98] [DeO97] [DeO98]. Therefore, new methods for structuring of the capacitors by chemical mechanical polishing (CMP) have recently been published [Sch00] [Iga00].

After patterning of the Pt and SBT layers by RIE, degradation of the electrical properties of the ferroelectric capacitors is observed. Several groups [Sai92] [Vij93] [Pan94] [Men96] reported reactive Ion Etching (RIE) of PZT thin film capacitors. The damage caused by the etching process can be recovered by an additional anneal (recovery or post anneal). After patterning and annealing well shaped hysteresis curves with low leakage currents are obtained. For PZT different wet cleaning methods for removing the sidewall redepositions or a secondary surface phase were reported which improved the electrical properties [Lee99a] [Lee99b] [Kim00] [Ran99] [Hor00]. Some work is published about RIE of SBT and its influence on electrical results [Des96] [Mae97] [Li00] [Asa99]. Electrical properties of SBT test capacitors in dependence of temperature and time for the recovery anneal are discussed. Also the effects of various annealing sequences are studied [Har98] [Eng99].

Although after patterning of platinum/crystalline-SrBi$_2$Ta$_2$O$_9$ bilayer by Argon based ion etching and high temperature annealing a recovery of electrical properties is seen for large capacitors, a degradation of the remanent polarization and leakage current of the capacitors with smaller feature sizes is observed. To
study the damage caused by the etching process to the SBT material itself, a set of blanket SBT layers (B-samples) was processed identically to the Pt/SBT/Pt capacitors (A-samples) except that no Pt top electrode is deposited and the SBT film is only partly etched (see Table 4). Structure analysis of the blanket SBT thin films after deposition, after crystallization anneal and after etching is performed with SEM, XRD and AES. It is shown that etching of crystalline SBT is damaging the SBT material, resulting in the formation of small crystallites (SEM), the appearance of an unknown peak (XRD) and reduction of the Bismuth content on the SBT surface (AES) [Har99] [Ahl99]. Using non-crystalline SBT, neither a degradation of electrical properties for smaller feature sizes nor a structural damage of blanket SBT is found after etching and recrystallization annealing although after etching of non-crystalline SBT also a loss of Bi is seen as indicated by AES. To explain the different results seen after patterning of crystalline and non-crystalline SBT material, a model will be proposed.

<table>
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</tr>
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</table>

Table 4: Process sequences of all samples produced for this study in this chapter. Electrical results of sample A9 will be reported in the entire chapter 6.2 and results of sample A10 in chapter 6.2.3 on page 95. Structural results of A- and B-samples will be reported in chapter 6.3 on page 96.

In Table 4 the process sequences for all samples produced for this study in this chapter are shown. A-samples have patterned capacitors with platinum top electrodes and B-samples are blanket SBT layers. For both set of samples, SBT layers with crystallization anneal and without crystallization anneal were produced. After patterning or etching of all samples, a high temperature anneal was performed. During the final anneal the samples with the non-crystalline SBT are crystallizing. A-samples were electrically characterized. The Pt/SBT/Pt capacitors of the A-samples were in the shape of squares with an area of 1000µm². For the measurements in chapter 6.2.3, capacitors in the shape of fingers with an area of 4000µm² were used. Contacting the bottom and top electrode of the capacitor was made possible via large Pt pads (see inset of Figure 44b on page 68 for a schematic drawing of the finger-shaped electrode with contact pad).
6.2. Electrical results of Pt/SBT/Pt capacitors after etching

6.2.1. Recovery anneals in oxygen

Best breakdown behavior of the Pt/SBT/Pt capacitors after patterning of Pt and SBT bilayer is obtained with Ar plasma after recovery anneal [Har98] [Eng99]. Therefore, all results presented are obtained after patterning with Ar plasma. All samples without recovery anneal after etching are shorted or very leaky (sample of type A7). Shorting or resistive leakage in virtual ground mode results in inflated curves in the polarization versus voltage plot with high apparent polarization values (see chapter 3.2 on page 31). No hysteresis loops are seen. In Figure 69 the evolution of these plots to typical hysteresis loops after recovery annealing at higher temperatures are shown (samples of type A9). The results underline how the shorted loops gradually evolve to the typical hysteresis loops. Only for recovery anneal temperatures higher than 600°C hysteresis loops are seen.

![Hysteresis Loops at Various Temperatures](image)

Figure 69: Evolution of the hysteresis loops before and after recovery anneals at 400°C up to 900°C of sample type A9. In virtual ground mode shorted or highly leaky capacitors result in inflated curves in the polarization versus voltage plot with high apparent polarization values. Typical hysteresis loops are only obtained for temperatures higher than 600°C.

However, the leakage current for the 600°C sample still is as high as $10^5$ A/cm$^2$ at 2V (Figure 70). Leakage currents lower than $10^7$ A/cm$^2$ at 2V are obtained for temperatures above 700°C. By plotting the logarithm of leakage current versus recovery anneal temperature an almost linear behavior is obtained.
The activation energy for the transformation of the capacitors from highly conductive capacitors to isolating capacitors is obtained by the use of the Arrhenius plot (Figure 70b). For the activation energy 0.51eV is obtained.

Figure 70: (a) Leakage current before recovery anneal and after recovery anneals at 400°C up to 900°C for samples of type A9. Performing the recovery anneal at temperatures lower than 600°C yields very leaky capacitors. (b) Arrhenius plot of the leakage currents of (a) for 400°C-900°C post anneal temperatures. For the activation energy 0.51eV is obtained.

Figure 71: Fatigue behavior after recovery anneal at different temperatures of sample type A9. Shorted or leaky samples can be recovered by electrical voltage cycling. (Polarization values >100 for the 500°C annealed sample are due to high leakage currents).
The influence of the recovery anneal on leakage current is studied for 1 - 60 min annealing time at 800°C in O₂ [Har98]. After 1 minute the leakage current drops from values higher than $10^{-3}$ A/cm² to $10^{-6}$ A/cm². However, leakage currents below $10^{-7}$ A/cm² are only obtained for times larger than 30 minutes. The increase in remanent polarization with longer annealing time is small.

Shorted or leaky samples of type A7 or A9 with a low temperature recovery anneal can be recovered by electrical voltage cycling (Figure 71). By applying a ±5V square pulse train to a 1000µm² capacitor with a frequency of 0.5MHz, polarization is decreasing for very leaky samples with a recovery anneal of ≤500°C and slightly increasing for samples with a recovery anneal of ≥600°C. For instance after $10^{10}$ cycles the hysteresis of a 500°C post annealed sample is restored from a bulky loop measured in virtual ground to a standard hysteresis loop (Figure 71).

![Figure 72: Polarization and leakage currents of sample types A8 and A10. Recovery annealing at 800°C in O₂ after patterning of Pt/non-crystalline-SBT layers, results in polarization values $2P_r$ of 5 µC/cm² and leakage currents >$10^{-7}$ A/cm².](image)

In Figure 72 the electrical results of non-crystalline SBT samples of type A8 and A10 are shown. Without a recovery anneal after patterning the non-crystalline SBT capacitors, only a paraelectric response with low leakage currents is obtained since no high temperature anneal up to this point is performed (A8). After recovery annealing at 800°C in O₂ of the patterned Pt/non-crystalline-SBT layers, now $2P_r$ polarization values of up to 5 µC/cm² and leakage currents of >$10^{-7}$ A/cm² are measured (A10).

In Figure 73 the effect of crystallization anneal and post anneal temperature on leakage currents are summarized.
6.2.2. **Low pressure recovery anneals**

After a 800°C crystallization anneal at atmospheric pressure, post anneals at 600°C, 700°C and 800°C are studied at 1.33mbar, 13.3mbar, 133mbar and at atmospheric pressure. For all temperatures studied only little changes in polarization are seen for all pressures and temperatures even for the 600°C post anneal. However, leakage currents for the 600°C and 700°C samples are significantly reduced by a low-pressure post anneal compared to an atmospheric post anneal (right side in Figure 73). Since the leakage currents of samples post annealed at 800°C are already in the $10^{-7}$ A/cm² range, leakage currents are almost the same or slightly higher with low-pressure post anneals.

For low pressure post anneals with temperatures identical to the SBT crystallization temperature of 675°C, 700°C, 725 °C and 800°C a different behavior is seen. This time no influence of the low pressure post anneal on leakage currents is observed (diagonal in Figure 73). Leakage currents are between $10^{-7}$ A/cm² and $10^{-6}$ A/cm² for 800°C annealed sample, between $10^{-6}$ A/cm² and $10^{-5}$ A/cm² for 725°C, around $10^{-5}$ A/cm² for 700°C and above $10^{-5}$ A/cm² for 675°C annealed sample. Therefore, leakage current seems to be only improved if low-pressure post anneal is done at temperatures lower than the crystallization temperature. Only little influence of low-pressure post anneal on polarization is observed either. For all pressures studied polarization values $2P_r$ of 10-12µC/cm² for 675°C, 13-14µC/cm² for 700°C, 15-16µC/cm² for 725°C and 18-19µC/cm² for 800°C are measured [Tri99].

![Figure 73: Effect of crystallization anneal and post anneal temperature on leakage current.](image-url)
6.2.3. Influence of dry etching on el. properties of crystalline and non-crystalline SBT films

For the electrical characterization of the samples in this chapter, Pt/SBT/Pt/Ti capacitors on SiO$_2$/Si wafers in the shape of fingers are used. Different capacitors with up to 128 fingers and a minimum width of 0.5µm are available. The area for all capacitors is 4000µm$^2$. Contacting the bottom and top electrode of the capacitor is made possible via large Pt pads (see inset of Figure 44b on page 68 for a schematic drawing of the finger-shaped electrode with contact pad).

In Figure 74a the remanent polarization $2P_r$ (normalized to the highest value of 15 µC/cm$^2$) and in Figure 74b the leakage current of sample A9 after etching of Pt/crystalline-SBT bilayer and post annealing in O$_2$ at atmospheric pressure are shown. On a semi-logarithmic plot, remanent polarization versus perimeter or width of fingers is almost decreasing linearly. Leakage current is increasing for smaller fingers or larger perimeters. Therefore, leaky zones at the perimeters of the capacitors after patterning of crystalline SBT and annealing must exist with degraded polarization values.

![Graphs showing polarization and leakage current versus perimeter](image)

Figure 74: (a) Polarization and (b) leakage currents versus perimeter of finger type capacitors after structuring of crystalline SBT capacitors and post annealing (sample of type A9). A decrease of the remanent polarization and a increase of the leakage current are seen.

However, after etching of Pt/non-crystalline-SBT bilayer and annealing of sample A10, an almost constant behavior versus perimeter is observed for both the remanent polarization (normalized to the highest value of 5 µC/cm$^2$) (Figure 75a) as well as the leakage current (Figure 75b). In this case no damaged edges at the perimeters of the capacitors should persist. But in general the absolute values for polarization and breakdown voltages are worse. Another drawback with patterning non-crystalline SBT capacitors is
arcing. As discussed in chapter 5.1, non-crystalline SBT is very smooth with very little z-range as measured by AFM (see Figure 45 on page 69). Therefore, the Pt/SBT/Pt wafer at the beginning of the dry etch process consists of one high-k dielectric capacitor. As evaluated in chapter 5.1, the probability to find one short on the entire wafer with non-crystalline SBT is very low whereas for the crystalline SBT the probability to find shorts is very high. Therefore, a highly isolating capacitor with non-crystalline SBT causes charging and then arcing in the plasma and on the wafer. Another consequence is that redepositions (e.g., formation of fences as usually seen after patterning with argon based plasma) after patterning of the capacitors are not responsible for the increase of the leakage currents of the crystalline sample A9 as shown in Figure 74, because etching of the non-crystalline sample A10 (as shown in Figure 75) did not show the degradation although for both samples the same etching process is used.

Figure 75: (a) Polarization and (b) leakage currents versus perimeter of finger type capacitors after structuring of non-crystalline SBT capacitors and post annealing (sample of type A10). Almost constant values for remanent polarization and no increase of the leakage current are seen.

6.3. Degradation mechanisms of Pt/SBT/Pt capacitors after etching

6.3.1. Study of Ar etch damage by SEM, AES and XRD

In Figure 76 the XRD measurements of a typical SBT module process flow are shown. The curves plotted are after SBT deposition and RTP, after crystallization anneal, after top electrode deposition, after top electrode etching and after recovery anneal. After crystallization anneal the (006), (111), (113) and (115) peaks of the SBT Aurivillius phase can be seen. Pt top electrode deposition does neither affect the SBT peaks nor a new peak is seen. However, after patterning an unknown peak appears at $2\theta = 27.5^\circ$. The ratio
of the area of this unknown peak to the area of the Aurivillius [115] peak reaches 22% after top electrode etching (Table 5, left column with numbers). After recovery annealing at 800°C, the ratio of the area of the unknown peak to the area under the Aurivillius [115] peak is reduced to 8%.

Another Pt/SBT/Pt/Ti/SiO$_2$/Si sample, which was not patterned shows after recovery anneal the same peak at 27.5°. For this case the ratio of this peak to the area under the Aurivillius [115] peak is 3%. The unknown peak is not present after top electrode deposition and before recovery anneal.

![XRD measurements](image)

**Figure 76:** XRD measurements after SBT deposition + RTP, after crystallization anneal, after top electrode deposition, after top electrode etching and after recovery anneal. Besides the peak for the layered perovskite, an unknown peak at $2\theta = 27.5^\circ$ after top electrode etching appears.

<table>
<thead>
<tr>
<th></th>
<th>ratio of peak areas (unknown peak / SBT[115])</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE deposition</td>
<td>0</td>
</tr>
<tr>
<td>top electrode etching</td>
<td>0.22</td>
</tr>
<tr>
<td>recovery anneal</td>
<td>0.08</td>
</tr>
</tbody>
</table>

**Table 5:** Ratio of the area under the unknown peak at 2$\theta = 27.5^\circ$ to the area under the Aurivillius [115] peak. Left column with numbers are taken from Figure 76 with etching the top electrode. Right column with numbers are taken from samples without etching the top electrode before performing the recovery anneal.

Blanket SBT films without Pt top electrode are produced to study the different behavior after etching of crystalline versus non-crystalline SBT material. The films are prepared as discussed in chapter 3.1 on page 27.
In Figure 77 the SEM pictures of the blanket SBT samples after deposition (B4), after crystallization anneal (B3), after Ar-etching of as deposited non-crystalline sample (B8), after Ar-etching of crystallized sample (B7), and after recovery anneal of Ar-etched non-crystalline SBT (B10) and crystallized SBT (B9) are shown. Please note etching of SBT films was done only partly in depth. The formation of small crystallites on the SBT surface after etching and annealing of the crystalline layer (sample B9) is clearly
visible whereas no new secondary phase is observed after etching and annealing of the non-crystalline SBT layer (B10).

In Figure 78 all XRD results of the corresponding crystalline (Figure 78a) and non-crystalline samples (Figure 78b) of Figure 77 are summarized. After crystallization anneal (sample B3) the (006), (111), (113) and (115) peaks of the SBT Aurivillius phase can be seen which are usually not seen directly after SBT deposition and RTP process (sample B4). However, after etching of the crystalline sample (B7) an unknown peak appears at $\theta = 27.5^\circ$ which stays after annealing (B9) but does not show up in the non-crystalline case (samples B8 and B10). Why the peaks typical for the Aurivillius phase show up after etching of the non-crystalline SBT layer although these peaks are not there before etching (sample B8), can be explained as following.

![XRD Intensity vs 2θ](image)

Figure 78: (a) XRD results of blanket crystalline SBT films (B3), after etching (B7) and etching + annealing (B9). After etching of crystalline SBT an unknown peak at $\theta = 27.5^\circ$ shows up. (b) XRD results of blanket non-crystalline SBT films (B4), after etching (B8) and etching + annealing (B10).

After SBT deposition, a RTP process step is performed. It was found (chapter 5.2.1 on page 71), that this RTP process step is crucial for obtaining high polarization values. Both temperature and ramp rate for RTP process are found critical. Studying the XRD results after this RTP process step from many wafers over a longer period of time, it is found that on a few wafers the typical peaks of the Aurivillius phase are found after RTP process step whereas on other wafers the typical peaks are not seen. The XRD result of sample B4 and B8 shown in Figure 78b originate from two different wafers, since etching of the wafers can only be done on whole wafers and not on wafer pieces, and for measuring wafers by XRD, wafers have to be broken and can not be reintroduced into the clean room environment. Therefore, fluctuations in ramp rate, temperature overshooting and so on are more likely the sources for the two different XRD
results of sample B4 and B8 and not the formation of the Aurivillius phase by the etching process (max. temp. 250°C). However, in contrast to the crystalline layer (B7) it is clear that the new peak is not seen at 27.5° after etching the non-crystalline SBT (B8).

Damaging of the SBT by etching is also seen by AES measurements. In Figure 79 the normalized AES data of the samples as shown in Figure 77 and summarized in Table 4 are plotted. After deposition (sample B4) and crystallization anneal (sample B3), Sr, Bi and Ta are found in stochiometric ratio. However, after etching a significant loss of Bi and increase of Ta compound are seen (B7 and B8). An increase of oxygen content on the SBT surface is also observed. This time there is no indication for a different behavior between crystalline and non-crystalline material. After etching and annealing (B9 and B10) surface compositions of both samples return almost to stochiometric ratios.

Figure 79: (a) AES results of blanket crystalline SBT films and (b) AES results of blanket non-crystalline SBT films: after deposition (B4), crystallization anneal (B3), etching of crystalline film (B7), etching of non-crystalline film (B8), etching + annealing of crystalline film (B9) and etching + annealing of non-crystalline film (B10). After etching a significant loss of Bismuth is observed for both set of samples.

6.3.2. Discussion and model

For the discussion of the results shown above, models will be proposed. One is to explain the decrease of the leakage currents after patterning and recovery annealing at high temperatures and the other is to explain the difference in the damaged area at the edge of the capacitor for crystalline versus non-crystalline SBT.

Leakage current versus temperature of recovery anneal
All samples with crystalline SBT but without a recovery anneal after top electrode deposition and patterning, are highly leaky or shorted. An explanation for this behavior is the filling of the voids in the SBT film by the fine grains of the platinum after top electrode deposition (Figure 80a). The filling of these voids at the interface between Pt top electrode and the SBT films interface for instance was already indicated by the AES result of the entire Pt/SBT/Pt/TiO\(_2\)/SiO\(_2\)/Si stack in chapter 4.3.1 (Figure 34b on page 57). The smaller slope of the Pt curve at the interface between the Pt top electrode and the SBT film (\(\alpha\)) compared to the slope of the Pt curve at the Pt bottom electrode (\(\beta\)) is an indication of penetration of fine grained as-deposited platinum in the SBT film from the top. This can cause a short between the top and bottom electrode. During recovery annealing Pt grains grow (Figure 15f on page 27). The larger crystallized Platinum grains can not fill the SBT voids (see Figure 80b) and lower leakage currents are measured after the recovery anneal. Consequently many voids are left at the Pt/SBT interface after recovery annealing due to Pt movement during Pt crystallization. Therefore, adhesion will also be lowered after recovery annealing (chapter 4.2.5, Figure 31, page 55).

![Figure 80: Proposed model for the morphological change of the interface of Pt/SBT (a) as-deposited and (b) annealed as shown in [Shi98a].](image)

The appearance of the unknown peak at \(2\theta=27.5^\circ\) after patterning of the Pt/SBT stack (Figure 76 on page 97) together with the AES results (Figure 79 on page 100) leads to the conclusion that etching causes the formation of a Bi-deficient SBT during patterning. However, due to the complexity of the Sr-Bi-Ta-O-Pt phase space, it was not possible to determine the exact phase from only one peak. Recovery annealing at 800\(^\circ\)C greatly reduces this unknown peak assumed to be a Bi deficient SBT. For other samples without patterning after top electrode deposition the same peak is observed (Table 5) but to much smaller extent. In

\[12\] Please note, that AES is only measuring the surface.
In this case, the unknown peak is caused by interaction of the top Pt with the underlying SBT layer at the Pt-SBT interface. Due to a reaction of the Pt electrode with residual Bi, a Bi-deficient SBT film in contact with a localized Bi-Pt alloy can be formed [Gut96] [Gut97]. Therefore, both at the edge of the capacitor as well as at the interface of the SBT to the Pt top electrode, a Bi deficient SBT is formed. For the edge of the SBT capacitor, the amount of Bi deficient SBT is highest after patterning and lowered by the high temperature recovery anneal. For the Pt/SBT interface, Bi deficient SBT is not present after Pt top electrode deposition but after high temperature recovery anneal. The activation energy for all these processes like Pt crystallization, formation of the Bi deficient SBT phase, formation of Pt-Bi alloy at increasing recovery anneal temperatures to lower the capacitor leakage, is 0.51eV.

The crystalline route

A7

Pt as dep.

crystl. SBT

Pt

A9

damaged zone

Pt as dep.

crystl. SBT

Pt

A10

Pt as dep.

crystl. SBT

Pt

The non-crystalline route

A8

Pt as dep.

non-crystl. SBT

Pt

A10

Pt as dep.

crystl. SBT

Pt

Figure 81: Proposed model of etching crystalline versus non-crystalline SBT capacitors. Patterning the Pt/SBT capacitors leads to a Bi deficient edge of the dielectric (samples A7 and A8). Due to the crystalline SBT, this damaged zone can not be recovered by the final recovery anneal (sample A9). For the non-crystalline SBT however, the Bi deficient regions at the edge are recovered during final anneal by the crystallizing SBT material itself (sample A10). The bismuth deficient layers at the interfaces to the bottom electrode (see chapter 4.3.4 on page 63) and to the top electrode due to interdiffusion of bismuth inside the Pt top electrode are not shown here.

It is also shown that shorted or leaky samples with a low temperature recovery anneal ≤600°C can be recovered by electrical voltage cycling (Figure 71). The same effect is observed after FGA (chapter 7). In all cases leaky paths along grain boundaries or at arcs of the rough Pt/SBT interface with high electric field intensity, are eventually burned off by heat being generated during the voltage cycling. Therefore, leakage current and polarization measured in virtual ground are decreasing after voltage cycling. Due to
the unpinning effect of domains, polarization is increasing for samples with recovery anneal $\geq 600^\circ\text{C}$ [Koh98].

Performing the recovery anneal at low pressure (e.g. 13mbar), lower leakage currents are obtained compared to a recovery anneal at atmospheric pressure (Figure 73) if the post anneal temperature is lower than the crystallization anneal temperature. Again, as discussed in 5.2.5, the coincidence of anneal pressure of 13mbar and the vapor pressure of Bi at 725°C of 14.3mbar, seems to be responsible for this effect.

For all samples with non-crystalline SBT without crystallization anneal and without recovery anneal after top electrode deposition and patterning, no shorts are measured in contrast to the samples with crystalline...
SBT. In this case the SBT layer consists of very small, dense and amorphous like SBT grains resulting in a paraelectric response and the lowest leakage current seen. Since no shorts are measured, although no recovery anneal after patterning is performed, redepositions, fence formation or other damages at the edge of the capacitor caused by the etching or patterning process cannot be responsible for any shorts. Therefore, as discussed above, the only way to produce a short for the crystalline SBT is through the SBT film with its voids. This is true because for both crystalline as well as for non-crystalline SBT the same dry etch plasma process is used. After recovery annealing of patterned Pt/non-crystalline SBT samples, SBT grains had grown and 2P values of 5µC/cm² are measured. However, leakage current, breakdown voltages and 2P values are worse compared to the sample where the crystallization anneal is carried out as usually before Pt top electrode deposition and etching.

**Damaged area at the edge of the capacitor**

It is shown that after patterning and annealing of the Pt/SBT stack by Argon based RIE, a degradation of the remanent polarization and leakage current of the capacitors for smaller feature sizes is observed. No degradation of electrical properties is seen after etching of non-crystalline SBT capacitors and annealing. To study the sidewall of the capacitors, etched blanket SBT films are used as a model experiment. Etching of crystallized SBT is damaging the SBT material, resulting in the formation of small crystallites (SEM), the appearance of an unknown peak (XRD) and reduction of the Bismuth content on the SBT surface (AES). Using non-crystalline SBT, neither a degradation of electrical properties for smaller feature sizes nor a structural damage of blanket SBT is seen after etching and re-crystallization annealing. However, for both cases a loss of Bi is seen after etching as indicated by surface sensitive AES. This Bi loss is recovered after final anneal for both cases.

It can be assumed that the small crystallites on the SBT surface after etching and annealing of the crystalline SBT correspond to the new peak as seen in XRD. The same unknown peak was also observed on non-patterned Pt/SBT/Pt/Ti/SiO₂/Si samples after final annealing (Table 5) [Har98]. Together with the AES results given, a Bi deficient SBT phase seems very likely.

Therefore, the following model is proposed: Patterning the Pt/crystalline-SBT/Pt capacitor leads to a Bi deficient edge of the dielectric. Due to the crystalline SBT, this damaged zone cannot be recovered by the final recovery anneal. For the non-crystalline SBT however, the Bi deficient edge regions are recovered during re-crystallization of the final anneal (Figure 81). The optical microscope pictures of capacitors of type A7-A10 after electrical breakdown correspond to the model proposed (Figure 82). Although the absolute values of the remanent polarization and breakdown voltages of the “non-crystalline” sample are worse compared to the sample where the crystallization anneal is carried out before, the different behavior
after etching as discussed above and its lower thermal budget could open new processes for integration issues of SBT capacitors.
7. Degradation mechanisms of SBT thin film capacitors in a hydrogen ambient

7.1. Introduction

Integration of the ferroelectric capacitor with advanced silicon Ultra-Large Scale Integration (ULSI) processes like tungsten plug deposition, interlayer dielectric (ILD) deposition, passivation deposition or forming gas anneal (FGA) requires major development. Especially the hydrogen rich backend of line (BEOL) processes endanger the functionality of the ferroelectric capacitor. Therefore, FGA is chosen as a model experiment to study the degradation mechanisms of SBT in a reductive ambient.

It is well known that H₂ annealing causes a severe change of the characteristics of the ferroelectric capacitor: polarization is reduced and leakage currents are increased by several orders of magnitude [Has97] [Kus96] [Han97] [Sim97] [Sak98]. For PZT, reduction of PbOₓ to its metallic state upon H₂ annealing was observed [Tak97a]. Metallic Pb can react with Pt to form a Pt-Pb alloy [Ika98] and grain boundaries become Pb deficient. The loss of lead and oxygen, the incorporation of hydrogen and the formation of [OH] bonds during FGA of PZT are described by S. Aggarwal et al. [Agg98]. For SBT, reduction of bismuth oxide to metallic bismuth [Koi98] and the formation of Pt-Bi compounds are seen [Bar98] [Har00b] [Har02] [Bos99]. Heavy peeling of the Pt/SBT/Pt capacitor after FGA was also reported [Zaf97]. A strong decrease of bismuth at the near surface region as a function of exposure to hydrogen and the formation of a thin amorphous non-ferroelectric layer was described by J. Im et al. [Im99]. Recovery of electrical properties in oxygen at higher temperatures is possible [Has97] [Sak98] [Kwo99], but for SBT it was found that recovery in air at 750°C is most ineffective if the FGA temperature was around Curie temperature [Agg99]. Many papers focus on the role of the top electrode in the degradation of the ferroelectric properties during FGA [Kus96] [Han97]. Due to the presence of noble metals like Pt, which act as a catalyst, molecular hydrogen is dissociated into atoms. The atoms react with the ferroelectric layer leading to reduced polarization and increased leakage currents. Using La₀.₅Sr₀.₅CoO₃ [Agg99] or other metals with less catalytic activity such as Au, Ag, Ni, Cu [Han97] [Sim97] [Fuj97] as a top electrode and the degradation during FGA can be prevented. Similar behavior is observed for iridium and ruthenium electrodes as well as for the respective oxide electrodes [Kus99] [Kus97] [Kan97] [Kat97]. To suppress the catalytic nature of platinum, incorporation of oxygen to the platinum top electrode has also been discussed in the literature. This can either be done by reactive sputtering of platinum with oxygen [Sae99] [Abe98] or simply by post annealing the top electrode [Fuj97]. Post anneal allows FGA at higher temperatures with less degradation of the ferroelectric properties [Fuj97]. However, in this study it was discovered that performing a post anneal after top electrode formation is responsible for the loss of
adhesion after FGA. Also, further degradation mechanisms of SBT films during FGA will be discussed. Specifically, the role of both the bottom and top electrode is analyzed.

7.2. Degradation of SBT films as seen by SEM and AES after forming gas annealing

Forming Gas Anneal of SBT/Pt/Ti/SiO₂ samples causes a dramatic change of the SBT surface (Figure 83a-c). Whiskers or needles and large crystals are observed on the SBT surface after FGA of crystalline SBT (Figure 83a). The length of the needles can reach up to a few μm and the size of the crystals up to 500nm.

Figure 83: SEM pictures of SBT surfaces and Pt surface after FGA: (a) crystalline SBT surface on Pt/Ti electrode after FGA. Whiskers as tall as several μm and large crystals are seen on the surface. (b) non-crystalline SBT surface
on Pt/Ti electrode after FGA. (c) SBTN surface on Pt/Ti electrode after FGA. (d) SEM picture of the Pt bottom electrode after removing the SBT layer. The whiskers as seen in (a) still remain, confirming that the whiskers originate from the bottom electrode.

Figure 84: AES element mapping (a) Ta, (b) Bi and (c) Pt, and (d) corresponding SEM picture of a SBT surface after FGA. Light area indicate high concentration of the analyzed species. The whiskers or crystals are free of Ta but rich in Bi and Pt.

In Figure 83b the SBT surface of a non-crystalline SBT sample after FGA is shown. In this case and for crystalline SrBi$_2$(Ta$_x$Nb$_{1-x}$)$_2$O$_9$ (SBTN) (Figure 83c) also tall whiskers are observed. However, the quantities of the whiskers are remarkably reduced. The main elements of the needles and crystals are Bi and Pt as determined by AES element mapping (Figure 84). The presence of Pt is indicating that the needles may originate from underneath the SBT layer. This is confirmed by etching off the SBT film using an HF-based solution (Figure 83d). The needles remain after the HF-based wets etch. After FGA of Pt electrodes without SBT, no needles are seen (not shown).
Due to the presence of platinum in the whiskers, the bottom electrode seems to play an important role in the formation of the protrusions on the SBT film after FGA. Use of thicker Pt electrodes usually results in a higher density of Pt hillocks after annealing of Pt/SiO$_2$ samples in O$_2$ (see Figure 27 on page 50, [Deh99] [Sha93] [Eri91]). Therefore, different platinum bottom electrodes with thicknesses of 100nm, 200nm and 300nm (all with an adhesion layer of 10nm Ti) are used to study the influence of the bottom electrode on the formation of the protrusions during FGA. However, no indication for an increased density of the Pt-Bi-needles and crystals with increasing Pt thickness is found (Figure 85b,c).

![Figure 85](image)

Figure 85: SEM pictures of SBT surfaces after FGA on (a) SiO$_2$, (b) Pt(100nm)/Ti(10nm) and (c) Pt(300nm)/Ti(10nm) substrates. Whiskers are only seen on Pt/Ti electrodes (b,c). The density of the Pt-Bi-whiskers does not depend on the thickness of the Pt/Ti bottom electrodes. Without platinum electrode no whiskers but Bi-crystals are seen. Please note the different scaling of picture (a) compared to pictures (b,c).

On other samples, SBT was deposited on SiO$_2$ directly without a platinum bottom electrode. In this case, no needles are seen but small crystals with a diameter of 100-500nm are observed (Figure 85a). The chemical composition of the crystals (labeled “crystal” in Figure 85a) and the area between the crystals (labeled “surface” in Figure 85a) are determined by AES element mapping. Ta and Sr are mainly found between the crystals (“surface” in Figure 85a) as expected from a typical SBT layer whereas only small amounts of Sr and Ta are seen in the crystals. However, a significant amount of Bi is observed in the crystals (Figure 86). In all cases bismuth signal is highest for the crystals and about 2.5 to 3 times higher than on a standard SBT surface without a FGA (reference in Figure 86).

The Bi$_3$ signal originates from a lower energy core level than the Bi$_1$ signal. This means that the penetration depth of the Bi$_3$ signal is higher. Therefore, using the Bi$_3$ signal Bi elements deeper underneath the surface can be detected. Since the Bi$_3$ intensity of the area called “surface” in Figure 85a is almost identical to the reference sample without a FGA (Figure 86b), the distribution of the bismuth underneath the surface did not change significantly after the FGA. However, the more surface sensitive
Bi1 signal is higher between the crystals after FGA ("surface" in Figure 85a) than on the reference sample (Figure 86a). Therefore, Bi(Oₓ) seems to accumulate on the SBT surface after FGA.

![Bi1 AES-Intensity](image1)

![Bi3 AES-Intensity](image2)

Figure 86: Result of AES B1 (a) and Bi3 (b) element mapping of the SBT layer of the SEM picture in Figure 85a. Two different crystals (labeled “crystal” in Figure 85a) and two different positions between the crystals (labeled “surface” in Figure 85a) are compared to a reference SBT surface without FGA. Bi1 signal is more surface sensitive.

7.3. HT-XRD, SIMS and FTIR analysis after forming gas anneal

In figure 87 the XRD spectra of a crystallized SBT thin film on a Pt/Ti electrode are shown. In-situ high temperature XRD measurements (see chapter 3.2 on page 35) are performed in forming gas. The position of the (006), (111), (113), (008) and (115) peaks for the SBT are unchanged. This means the ferroelectric Aurivillius phase of SBT is not damaged crystallographically up to approx. 500°C in forming gas. However, the intensity of the (115) and (113) peaks are gradually decreasing, indicating a gradual decrease of SBT crystallinity. New peaks, however, are only seen at 550°C and higher. Therefore, a change of SBT to a new phase occurs around 550°C. This phase could not be determined yet. Between 700°C and 750°C the newly developed phase disappears and the SBT layer becomes completely amorphous.

The diffusion and accumulation of the hydrogen during FGA was investigated by SIMS (see page 38). However, there are several issues to be faced. One is the limited detection of hydrogen by the SIMS technique due to the fact that hydrogen is found naturally in the air in the form of H₂O and therefore it is present on the sample as well as inside the chamber. To differentiate natural hydrogen from hydrogen from the FGA, a FGA is used in which the hydrogen is substituted by the isotope deuterium [Gil99]. Samples are annealed in a mixture of 5% D2 and 95% N2. The other issue is peeling of the top electrode
after FGA making a SIMS analysis impossible. To avoid peeling, a silicon oxide layer was deposited on top of the capacitor stack. The silicon oxide prevents the heavy peeling, but does not stop the diffusion of the deuterium.

![SBT/Pt/Ti under N2/H2 flow](image)

**figure 87:** High temperature XRD scans of a SBT/Pt/Ti sample under constant flow of forming gas.

![Secondary Ion Intensity](image)

**figure 88:** SIMS profiles of SiO$_2$ capped Pt/SBT/Pt/Ti/SiO$_2$ samples before and after deuterated FGA (95% N$_2$, 5% D$_2$). The accumulation of deuterium (H2-signal) inside the SBT layer after the anneal is clearly seen.

The SIMS results before and after deuterated FGA at 430°C$^{13}$ of SiO$_2$ capped Pt/SBT/Pt/Ti/SiO$_2$ samples are shown in figure 88. After FGA with deuterium the D$_2$-level is increased significantly with deuterium

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$^{13}$ The deuterium level of a non-annealed pure Ti sample is up to four orders of magnitude under the hydrogen level. This result is expected since it corresponds to the natural composition of hydrogen and deuterium in air.
seen inside the SBT layer and at platinum interfaces next to the SBT. This clearly shows that deuterium (or hydrogen) is diffusing or accumulating preferably inside the SBT layer and the Pt layers next to it. Whether the hydrogen is accumulating within the SBT grains or at the SBT grain boundaries has yet to be determined. Taking into account that the HT-XRD data showed no degradation of the SBT phase up to approx. 500°C in forming gas, it is very likely that the hydrogen or deuterium is accumulated mainly in the grain boundaries.

FTIR (Fourier Transform Infrared) analysis of Pt/SBT/Pt/Ti/SiO$_2$ samples after FGA are performed to check for OH-bonds in the range from 3600-3000cm$^{-1}$. However, neither OH- nor PtH-bonds are seen. Therefore, hydrogen does not react with SBT to form OH-bonds or the amount of OH-bonds is under the detection limit of 1%.

7.4. Influence of the Pt top electrode and anneal steps post Pt top electrode formation

As already mentioned in the introduction of chapter 7.1, the catalytic influence of the top electrode was studied in detail by other groups. Here the effect of annealing sequences post top electrode formation are discussed.

![Image of Optical microscope pictures](image_url)

Figure 89: Optical microscope pictures of (a) Pt/SBT/Pt sandwich after high temperature anneal in O$_2$ and after FGA, and (b) a IrOx film after FGA. The Pt top electrode (a) and the IrOx film (b) are peeling off almost entirely.

It is found that for FGA of a Pt/SBT/Pt/Ti/SiO$_2$ sample, two different cases have to be compared. After patterning of the platinum top electrode, typically a high temperature post anneal in oxygen is performed to recover the damage caused by the etching process [Hart98] [Hart99] and to crystallize the top electrode
to smooth the Pt/SBT interface to obtain capacitors without shorts [Shi98a]. Performing FGA on these annealed samples results in a major damage of the capacitors and massive peeling of the top electrodes (Figure 89a). However, after FGA of a Pt/SBT/Pt/Ti/SiO$_2$ sample without such a HTA step, no peeling is observed.

To study the difference observed, blanket Pt layers were deposited directly on SiO$_2$ as a model experiment for measuring the residual stress of the platinum electrodes after each annealing step. Although adhesion of platinum is normally poor on SiO$_2$, only the results of this type of samples are reported here since Pt/Ti/SiO$_2$ samples show identical results and peeling was never observed for either type of samples. This was also checked by tape test before and after FGA. Platinum deposition on SiO$_2$ is done at 190°C, 300°C and 550°C.

Figure 90: Pt electrodes deposited at different temperatures on SiO$_2$. Residual stress after deposition, after high temperature annealing in O$_2$, after annealing in N$_2$ and after FGA are shown.

Figure 91: Pt lattice spacing calculated from Pt(222) XRD peaks for different anneal cycles.

As seen in Figure 90 (labeled “as dep.”), residual stress is increasing with deposition temperature of the platinum. The tensile stress is generated during cooling due to the difference of the thermal expansion coefficients of Pt ($9.0 \times 10^{-6}$ 1/K) and Si ($2.6 \times 10^{-6}$ 1/K) (see also chapter 4.2.3 and Figure 25 on page 46). Deposition temperature does no longer have any effect on stress after annealing the samples at 800°C in dry oxygen (labeled “after 800°C,O$_2$” in Figure 90). All electrodes show almost identical tensile stress of around 0.8 GPa. FGA at 430°C causes a decrease of overall stress of up to 20% (labeled “after 800°C,O$_2$ + FGA” in Figure 90). For comparison, other samples are annealed in pure N$_2$ at 430°C after the 800°C anneal in dry oxygen (labeled “after 800°C,O$_2$ + N2” in Figure 90). Unlike the samples annealed in FGA, almost no change of stress is measured for the pure N$_2$ annealed samples. FGA carried out directly after
platinum deposition at 550°C without an intermediate HTA shows almost no change of stress (labeled “after FGA” in Figure 90). For electrodes deposited at 190°C and 300°C an increase of stress to values similar for platinum deposited or annealed at 430°C is observed. These findings are confirmed by measuring the lattice constants of Pt. Measured differences in lattice constants can be correlated directly to the strain. Pt(222) diffraction peaks are precisely measured [Har02]. The peak position for the Pt sample annealed at 800°C is shifting to a higher angle compared to the as deposited Pt sample. Therefore, the lattice constant of the Pt film is shrinking (Figure 91). However, as indicated already by the residual stress measurements, platinum lattice spacing is expanding after 800°C anneal plus FGA.

7.5. Discussion and model

Influence of the bottom electrode

From the results shown above, the following model for degradation of the SBT/Pt/Ti/SiO₂ stack is proposed. During high temperature crystallization anneal in oxygen of the as deposited SBT film on Pt/Ti(Oₓ)/SiO₂, Bi(Oₓ) and oxygen are diffusing into the bottom electrode (see chapter 4). There, oxygen and Bi(Oₓ) reacts with TiOₓ (TiOₓ is formed in the Pt/Ti bottom electrode after the first electrode anneal) to form BiTiOₓ (see Figure 40 on page 62). During FGA, hydrogen - promoted by the catalytic nature of Pt - reduces BiOₓ to its metallic form. Since the near grain boundary volume of SBT mainly contains excess bismuth oxide remaining from the crystallization process [Gut96] [Koi97], elemental bismuth is created at the SBT near grain boundary volume by reducing bismuth oxide. Elemental bismuth will be found at the near grain boundary volume, on the SBT surface and at the interface to the bottom electrode. Since the temperature of the FGA is above the melting point of bismuth of 217°C (see Figure 10 on page 19), this very mobile, liquid bismuth metal is alloying with the platinum. With the platinum layer and the SBT film as an almost inexhaustible source for Pt and Bi, Pt-Bi needles or crystals can grow through the SBT film and even a few microns higher (Figure 92b).

Less Bi in the as-deposited film would also leave less bismuth at the near grain boundary volume. Therefore, a near grain boundary volume containing only little bismuth would be less sensitive to hydrogen [Kan97] but usually give much lower polarization values due to the formation of pyrochlore phase. Also, less Bi diffused from the SBT layer into the Pt bottom electrode should give less Pt-Bi whiskers as seen on non-crystalline SBT/Pt/Ti/SiO₂ samples (see Figure 83b) compared to crystalline SBT/Pt/Ti/SiO₂ samples (see Figure 83a). Since for the crystalline SBTN samples only few whiskers are seen either (see Figure 83c), it can be concluded, that for the crystalline SBTN sample diffusion of Bi into the Pt bottom electrode is lower than for the SBT sample. This could also be one of the reasons why higher polarization values are usually seen for standard processed SBTN compared to standard SBT.
Also, bismuth can diffuse from inside the SBT grain to the near grain boundary volume [Poo00]. As shown above, the Bi3 signal originates not only from the surface but also from layers underneath. For this signal no difference between the SBT surface after FGA and the surface from a reference SBT sample without FGA is found (see Figure 86b). However, diffusion of bismuth from inside the SBT grain should result in a different Bi3 signal as compared to a reference SBT surface without a FGA. This together with the fact that the SBT phase is stable up to approx. 500°C in forming gas (see XRD result in figure 87) shows that diffusion of bismuth from inside the SBT grain to the near grain boundary volume is only minor for the FGA at 430°C.

The thicker the platinum electrode the more hillocks are usually observed after annealing of Pt/SiO₂ samples in O₂. However, after FGA of SBT/Pt/SiO₂ samples, no clear indication for the dependence of the density of the Pt-Bi-whiskers on the platinum thickness is obtained. Therefore, the assumption that the hillocks of the platinum bottom electrode act as seed spots for the growth of the Pt-Bi whiskers does not appear to be valid.

The metallic whiskers, crystals or Pt-Bi rich grain boundaries are responsible for shorting the Pt/SBT/Pt capacitor after FGA. As reported, leakage or shorting can be recovered by annealing in an oxygen atmosphere after FGA [Has97] [Sak98] [Kwo99] [Shi99]. During the oxygen anneal, oxygen is incorporated into the ferroelectric film to recover the oxygen vacancies created by the FGA [Has97]. With the removal of these oxygen vacancies or charge traps, domain wall pinning does not occur anymore and a higher remanent polarization is obtained. During the HTA it is also very likely that the mobile Pt-Bi compounds - formed after the FGA mainly at the near grain boundary volume - recrystallize first to BiₓPtOᵧ and then to SBT and Pt [Shi99] and migrate to the bottom and top electrodes. It is reported, that high leakage currents can be recovered by electrical cycling [Cha99] [Hon00]. In this case, the heat being
generated eventually burns off shorts or leakage paths at the SBT grain boundaries caused by the Pt-Bi compounds. Therefore, no shorts and low leakage currents are observed after HTA or cycling. Without a platinum bottom electrode metallic bismuth - mainly from the near grain boundary volume - is crystallizing to Bi rich crystals and a thin Bi rich layer on the surface upon cooling (Figure 92a).

**Influence of the top electrode**

For the degradation of the Pt/SBT/Pt/Ti/SiO$_2$ stack the following model is proposed. Sputtering the top electrode results in small Pt grains (Figure 93a). High temperature annealing (HTA) induces grain growth in the platinum top electrode (Figure 93b). Cooling to RT leads to an increase of the tensile stress due to the difference of the thermal expansion of Pt and Si.

(i) It was shown that performing a FGA after the HTA leads to a decrease of the residual stress (Figure 90). It is known that a change of stress can affect the ferroelectric properties. Polarization or dielectric properties can change [Sha99] as soon as stress distorts the lattice. However, with respect to the peeling discussed above, the small decrease of stress would actually help to relief some of the stress being stored in the Pt film and should not cause any peeling. Therefore, other possible degradation mechanisms for peeling of annealed Pt/SBT/Pt-samples after FGA have to be considered.

(ii) As discussed by Y. Fujisaki [Fuj97] and C. S. Hwang [Hwa99], platinum grain boundaries get partially oxidized during HTA in oxygen. Partially oxidized Pt grain boundaries would lead to an expansion of the Pt layer and therefore to a slight decrease of stress. However, the difference of the thermal expansion of Pt and Si is overcompensating this expansion and still resulting in an increase of total stress after HTA. We found that performing a HTA step in pure nitrogen, no counteracting expansion of oxidized Pt grain boundaries is obtained and therefore the residual stress becomes even slightly higher. For the sample annealed in O$_2$ it is likely that during FGA the partially oxidized platinum grain boundaries are being reduced to their metallic form. As reported [Gme86], platinum dioxide is easily reduced by gaseous hydrogen. This could lead to peeling of the top electrode. For comparison, a FGA of an IrO$_x$ layer was performed. In this case an almost entire loss of adhesion after FGA is observed (Figure 89b). Reduction of IrO$_x$ to its metallic state during FGA [Kus99] may cause the peeling. The same may be valid for PtO$_x$.

(iii) A chemical reaction of platinum, hydrogen and the SBT film during FGA is probably more likely to cause the degradation. Reactions like reducing bismuth oxide to its metallic form and alloying to Pt-Bi as discussed above can cause the peeling of the platinum film. Since the sample without a HTA step did not show any peeling after FGA, the existence of a high tensile stress in the platinum film seems to be mandatory to cause peeling after FGA. Another important factor taken into account is hydrogen diffusion. Due to the large and columnar structure of Pt grains after HTA of the Pt top electrode, hydrogen is believed to diffuse more easily to the Pt/SBT interface [Has97] to initiate reactions between SBT and Pt.
(Figure 93b). In contrast, the small and dense structure of Pt grains after deposition without HTA does not allow fast hydrogen diffusion along grain boundaries and therefore no peeling after FGA is observed (Figure 93a). Therefore, whenever platinum films with high tensile stress after HTA see a reducing ambience like FGA, ILD deposition or W deposition, loss of Pt top electrode adhesion may occur.

![Diagram](image)

Figure 93: Proposed model: (a) After SBT crystallization anneal, large SBT and platinum grains of the bottom electrode are left. Sputtering top electrode leaves only small Pt grains. (b) During high temperature annealing in oxygen after patterning the capacitor, Pt grains grow. FGA causes peeling of the top electrode for the later case whereas no peeling is observed for the former one.
8. Conclusions and summary

Ferroelectric random access memories (FeRAMs) are new types of memories especially suitable for mobile applications due to their unique properties like non-volatility, small DRAM-like cell size, fast read and write as well as low voltage/low power behavior. Although standard CMOS processes can be used for frontend and backend/metalization processes, FeRAM technology development has to overcome major challenges due to new materials like Pt and SrBi$_2$Ta$_2$O$_9$ used for capacitor formation. The most important processes are Pt bottom electrode formation and its interaction with the ferroelectric layer SBT, thin film ferroelectric layer deposition and crystallization control, Pt top electrode patterning and recovery anneal, and finally the backend of line (BEOL) processes. The bottom electrode processes like deposition temperature, thickness, anneal sequence and the chosen pre layer stack, are very critical to the performance of the ferroelectric capacitor because the bottom electrode is present during the high temperature crystallization anneal of the following ferro layer. Interactions like interdiffusion or crystallization between the ferro layer and the bottom electrode influence the Pt-SBT interface and therefore the electrical results. The crystallization anneal after deposition of the ferro layer determines the grain size, the morphology and overall electrical characteristic of the capacitor. To heal the structural damages after top electrode patterning, a recovery anneal is necessary. And finally, the hydrogen rich process in the BEOL can reduce the oxides in the ferroelectric and destroy the layer.

Bottom electrode

Pt/Ti and Pt/TiO$_x$ bottom electrodes for ferroelectric SrBi$_2$Ta$_2$O$_9$ (SBT) thin films have been studied. Microstructural analysis by Auger Electron Spectroscopy (AES), Transmission Electron Microscopy (TEM), Scanning Electron Microscopy (SEM), stress-temperature and sheet resistance measurements clearly show the diffusion and oxidation of Ti inside the platinum electrode. It is found, that Ti diffusion of a 20nm Ti layer stops roughly 50nm underneath the platinum surface regardless the thickness of the platinum layer of 100, 200 and 300nm. It is shown that by using Pt/TiO$_x$ bottom electrodes higher polarization values compared to Pt/Ti bottom electrodes are obtained. Variations of the electrode system by using different thickness for Pt/Ti and Pt/TiO$_x$ clearly show: The higher the ratio of the Ti thickness versus the Pt thickness the lower the polarization values and the higher the coercive voltage of the corresponding hysteresis loop. The formation of interfacial TiO$_x$ layer could explain the differences seen by assuming two series capacitors with the interfacial layer having a lower dielectric constant. However, a TiO$_x$ layer between the Pt/Ti bottom electrode and the SBT layer can be neglected since no Ti is found by AES above the Pt surface. Doping of the SBT layer with Ti from the Pt/Ti bottom electrode can be neglected for the same reason because it is shown that for degradation of the electrical properties as seen, an incorporation of Ti inside the SBT of more than 1% is needed which is not seen by AES. Consequently,
incorporation of Ti inside SBT is not the root cause for the lower polarization values of Pt/Ti electrodes either. Therefore, a new model is proposed.

By calculating the Bi loss (ratio of bismuth content after wet chemical etching of SBT layer on Pt electrode and bismuth content after SBT coating and crystallization anneal) by using Total X-Ray Fluorescence (TXRF) technique, the loss of bismuth into the Pt electrode is found to be almost 40% higher for Pt/Ti electrodes compared to Pt/TiOx electrodes (for the Pt/TiOx electrode, the Ti was oxidized prior to the Platinum deposition). This difference in Bi-loss could result in different crystallization of SBT at the Pt-SBT interface. For the Pt/Ti electrode the formation of Bi-deficient SrO-Ta2O5 with a lower dielectric constant at the interface could explain the higher polarization values for Pt/TiOx electrodes compared to Pt/Ti.

The critical parameters identified for hillocks grow in Pt bottom electrode are: sputter deposition temperature, thickness, annealing temperature and the substrate used. For Pt adhesion the critical parameters are identical except that adhesion seems to be independent of the Pt thickness.

To evaluate the model proposed for the explanation of the higher polarization values for Pt/TiOx electrodes compared to Pt/Ti by the higher Bi loss, the Bi loss of SBT on Pt/Ti versus Pt/TiOx for different SBT thickness should be measured by TXRF. Also, the production and electrical characterization of capacitors with different ultra thin SBT on Pt/Ti versus Pt/TiOx would help verifying the model. It is also known that doping of SBT by Nb gives much larger SBTN grains and higher polarization values. These results may be revisited by the determination of the Bi loss and a possible interfacial layer.

SBT layer

Thin films of SBT were deposited on Pt/Ti/SiO2/Si substrates using MOD (Metal-Organic Decomposition) two layer spin-on processing. The films were annealed at 800 °C in diffusion furnace under flowing O2 for complete crystallization. It was found that the grain growth could be enhanced; leading to improved ferroelectric properties, by introducing a two-step anneal methodology. The first step involves rapid thermal processing (RTP) of the SBT layers at temperatures close to 700 °C for 30s at ramp rates between 75 to 125°C/s followed by the second anneal employing a diffusion furnace at 650-800 °C for 30 to 60min. This RTP step promotes grain growth by creating nucleation sites. After the diffusion anneal larger grains, more SBT clusters and less porosity are seen compared to samples without the additional RTP step. Annealing the SBT above crystallization temperature, SBT film thickness decreases with temperature and refractive index increases due to crystallization of SBT. The higher the crystallization temperature the larger the SBT grains and the higher the polarization values. The thinner the SBT films the more secondary phases are seen which result in an increase of refractive indexes. At 800°C crystallization anneal SBT grains are largest and its structure is almost independent of the film
thickness since the temperature is well above the initial crystallization temperature. The large grains with voids at higher crystallization temperatures are responsible for shorts in SBT films <120nm. To reduce the chance of oxidation of the poly-silicon plug underneath the bottom electrode for vertical high density FeRAMs with stack cells, low-pressure crystallization and nitrogen anneals were studied. For low pressure anneals the best pressure range is determined by the vapor pressure of Bi at the desired temperature. For pressures well below the vapor pressure of the Bi only low polarization values are obtained. SBT films get highly Bi deficient leading to incomplete crystallization and therefore to low polarization values. Low-pressure Pt/Ti bottom electrode experiments showed that oxygen supply during anneal at pressures <0.1mbar is not sufficient either since Ti could diffuse even to the top of the Pt electrode. Therefore, evaporation of Bi and low oxygen supply at crystallization anneals <0.1mbar cause degradation of the ferroelectric properties for pressures well below the vapor pressure of the Bi. For pressures around the vapor pressure of the Bi higher polarization values were obtained than at atmospheric pressure. This is assumed to be due to some depletion of residual metallic bismuth after sub atmospheric pressures anneals. Metallic Bi left over at the near grain boundary volume may pin the domain walls, which will result in lower polarization values.

The best process sequence with nitrogen anneals is as follows: pre anneal in O$_2$, RTP and crystallization anneal in N$_2$ and the post anneal in O$_2$. Performing the pre anneal or electrode anneal in nitrogen, leads to diffusion of titanium up to the platinum surface and poisons the ferroelectric layer after deposition of SBT. After SBT coating, the organics in the MOD film have to be burned off first at lower temperatures in oxygen followed by a high temperature RTP step in nitrogen. A crystallization anneal in nitrogen does not alter the ferroelectric properties either. However, post anneal in nitrogen after capacitor formation leads to slightly lower polarization values, higher leakage current and higher fatigue characteristics. Post anneal in oxygen seem to be necessary to recovery the damages after patterning.

**Capacitor patterning and recovery**

It has been shown that after patterning of the Pt/SBT stack no hysteresis loops are obtained without recovery anneal. Hysteresis loops are only obtained for recovery temperatures T ≥ 600°C. However, to yield low leakage currents of ≤ 10$^{-7}$ A/cm$^2$, recovery annealing temperatures T > 700°C are necessary. It has also been shown that after patterning and annealing of the Pt/SBT stack by Argon based RIE, a degradation of the remanent polarization and leakage current of the capacitors for smaller feature sizes is observed. No degradation of electrical properties is seen after etching of non-crystalline SBT capacitors and annealing. The following model is proposed. For both crystalline SBT as well as non-crystalline SBT, a damaged edge around the capacitor is created after structuring, which is mainly Bi deficient SBT. Due to the crystalline SBT with many voids and the as-deposited Pt with small grains, all capacitors without recovery anneal are shorted. On the other side no shorts are detected on samples with non-crystalline SBT.
due to its dense structure. After annealing of patterned crystalline SBT, the Bi loss at the edge of the capacitor cannot be recovered due to the crystallinity of the SBT. Therefore, Bi from the near grain boundary volume of the crystalline SBT away from the edge is trying to compensate for the Bi loss at the edge of the capacitor as conformed by AES on blanket crystalline SBT samples. A damaged zone with Bi deficient near grain boundary volume is left, leading to the degradation of the electrical properties at smaller feature sizes. Also, during the recovery anneal the Pt grain size of the top electrode is increasing and no shorts are observed anymore. For the non-crystalline material the situation is different. In this case the non-crystalline material can compensate the Bi loss during the crystallization process of the anneal. No Bi-deficient near grain boundary volume and no damaged zone is left. No degradation of the electrical properties at smaller feature sizes is observed.

**Degradation of capacitors in a H\(_2\) environment**

The effects of annealing in forming gas (5% hydrogen, 95% nitrogen; FGA) were studied. SBT films on platinum bottom electrode were characterized with and without platinum top electrode. Films were characterized by residual stress measurements, Scanning Electron Microscopy (SEM), Auger Electron Spectroscopy (AES), High Temperature X-Ray Diffraction (HT-XRD) and Secondary Ion Mass Spectrometry (SIMS). HT-XRD of blanket Ti/Pt/SBT films in forming gas revealed that the bismuth layered perovskite structure of SBT is stable up to approx. 500°C. After formation of an intermediate phase between 550°C and 700°C, SBT changes its structure to an amorphous phase. SIMS analysis of Pt/SBT/Pt samples annealed in deuterated forming gas (5% D\(_2\), 95% N\(_2\)) showed that the hydrogen accumulates in the SBT layer and the platinum interfaces next to the SBT. After FGA of blanket SBT films, tall platinum-bismuth whiskers are seen on the SBT surface. It is confirmed that these whiskers originate from the platinum bottom electrode and grow through the SBT layer. FGA of the entire Pt/SBT/Pt/Ti stack shows two different results. For the samples with a high temperature annealing step in oxygen after top electrode patterning, peeling of the top electrode is observed after FGA. For the samples without a high temperature annealing step, no peeling is observed after FGA. Therefore, the existence of a high tensile stress in the platinum film after HTA combined with large, columnar Pt grains seems to be mandatory to cause peeling after FGA. Also, Platinum films under tensile stress after HTA and a chemical reaction of platinum, SBT and hydrogen during FGA cause the degradation. Therefore, whenever platinum films with high tensile stress and large columnar grains after HTA see a reducing ambience such as FGA, W-CVD deposition and ILD deposition, loss of Pt top electrode adhesion may occur. Annealing sequence, stress of Pt layer and chemical reactions of platinum, SBT and hydrogen seem to play important factors in the degradation mechanisms of Pt/SBT/Pt capacitors during FGA.
Besides peeling, poor electrical properties of the ferroelectric capacitor (FeCAP) are a consequence of hydrogen rich processes. To protect the capacitor from the observed damage by hydrogen an Encapsulation Barrier Layer (EBL) is needed. There are many materials like AlO$_x$ [Par97], TiN [Has97], TiO$_x$ [Kud97], SiON [Nak99], SiN [Har00a] and ZrO$_x$ [Kas99] proposed for the use as a hydrogen barrier.
9. Appendix

References


[Har00e] W. Hartner, Z. Gabric, G. Schindler, filed Infineon invention 100 41 685.3 or 100 01 118.7, (2000)
### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>1T/1C</td>
<td>One Transistor / One Capacitor Cell</td>
</tr>
<tr>
<td>AES</td>
<td>Auger Electron Spectroscopy</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
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<tr>
<td>BEOL</td>
<td>Back-End of Line</td>
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<tr>
<td>BL</td>
<td>Bit Line</td>
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<tr>
<td>BST</td>
<td>Barium Strontium Titanate (Ba&lt;sub&gt;x&lt;/sub&gt;Sr&lt;sub&gt;1-x&lt;/sub&gt;TiO&lt;sub&gt;3&lt;/sub&gt;)</td>
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<tr>
<td>BTO</td>
<td>Bismuth-Titanate (BiTi&lt;sub&gt;y&lt;/sub&gt;O&lt;sub&gt;y&lt;/sub&gt;)</td>
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<tr>
<td>CFeRAM</td>
<td>Chain Ferroelectric Random Access Memory</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
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<tr>
<td>CMP</td>
<td>Chemical Mechanical Polishing</td>
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<tr>
<td>CMVP</td>
<td>Capacitor on Metal via Stacked Plug</td>
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<tr>
<td>CSD</td>
<td>Chemical Solution Deposition</td>
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<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
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<td>DC</td>
<td>Direct Current</td>
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<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
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<tr>
<td>DRO</td>
<td>Destructive Read Out</td>
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<tr>
<td>EBL</td>
<td>Encapsulation Barrier Layer</td>
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<tr>
<td>EDX</td>
<td>Energy Dispersive X-ray</td>
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<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read Only Memory</td>
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<tr>
<td>EPROM</td>
<td>Erasable Programmable Read Only Memory</td>
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<td>F</td>
<td>Minimum Feature Size</td>
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<td>FeA</td>
<td>Ferro Anneal</td>
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<td>FEOL</td>
<td>Front-End of Line</td>
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<tr>
<td>FeRAM</td>
<td>Ferroelectric Random Access Memory</td>
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<tr>
<td>FGA</td>
<td>Forming Gas Anneal</td>
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<tr>
<td>FRAM</td>
<td>Ferroelectric Random Access Memory (registered trademark by Ramtron Corp.)</td>
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<tr>
<td>FTIR</td>
<td>Fourier Transform Infrared</td>
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<td>GOI</td>
<td>Gate Oxide Integrity</td>
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<td>HTA</td>
<td>High Temperature Anneal</td>
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<td>High Temperature X-Ray Diffraction</td>
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<tr>
<td>ICP</td>
<td>Inductively-Coupled Plasma</td>
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<td>ILD</td>
<td>Interlayer Dielectric</td>
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<td>k</td>
<td>Dielectric Constant</td>
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<td>Abbreviation</td>
<td>Definition</td>
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<tr>
<td>LOCOS</td>
<td>Local Oxidation of Silicon</td>
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<td>LSMCD</td>
<td>Liquid Source Mist Chemical Deposition</td>
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<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
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<td>Magnetically Enhanced Reactive Ion Etching</td>
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<td>MFS-FET</td>
<td>Metal-Ferroelectric - Semiconductor Field Effect Transistor</td>
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<tr>
<td>MOD</td>
<td>Metal Organic Decomposition</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>NDRO</td>
<td>Non-Destructive Read Out</td>
</tr>
<tr>
<td>NO</td>
<td>Nitride / Oxide</td>
</tr>
<tr>
<td>PL</td>
<td>Plate Line</td>
</tr>
<tr>
<td>PLD</td>
<td>Pulsed Laser Deposition</td>
</tr>
<tr>
<td>PoA</td>
<td>Post Anneal</td>
</tr>
<tr>
<td>PrA</td>
<td>Pre Anneal</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical Vapor Deposition</td>
</tr>
<tr>
<td>PZT</td>
<td>Lead-Zirconium-Titanate (PbZr$_{1-x}$Ti$_x$O$_3$)</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
</tr>
<tr>
<td>RT</td>
<td>Room Temperature</td>
</tr>
<tr>
<td>RTP</td>
<td>Rapid Thermal Processing</td>
</tr>
<tr>
<td>SBT</td>
<td>Strontium-Bismuth-Tantalate (SrBi$_2$Ta$_2$O$_9$)</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectroscopy</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integrated Circuits</td>
</tr>
<tr>
<td>WL</td>
<td>Word Line</td>
</tr>
<tr>
<td>XPS</td>
<td>X-Ray Photoelectron Spectroscopy</td>
</tr>
<tr>
<td>XRD</td>
<td>X-Ray Diffraction</td>
</tr>
<tr>
<td>XRF</td>
<td>X-Ray Fluorescence Spectroscopy</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>dielectric constant</td>
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</table>
List of own papers (author and co-author)


"Integration of H$_2$ Barriers for Ferroelectric Memories Based on SrBi$_2$Ta$_2$O$_9$ (SBT)", W. Hartner, G. Schindler, P. Bosk, Z. Gabric, M. Kastner, G. Beitel, T. Mikolajick, C. Dehm. and C. Mazuré, Integrated Ferroelectrics 31, 273 (2000)


Curriculum Vitae

- Name: Walter Hartner
- Personal: Born on January 2nd 1968 in Lauingen/Donau, Germany
  Married, 2 daughters

- 1987 Abitur at the St. Bonaventura Gymnasium in Dillingen/Donau, Germany
- 1989-1995 Study of Physics at the Friedrich-Alexander Universität in Erlangen, Germany
- 1995 Graduation - Diploma-Thesis "Study of Silicon Carbide (SiC) Surfaces by Scanning Tunneling Microscopy (STM)" at the Solid State Institute under Prof. Dr. Müller and Prof. Dr. K.Heinz at the Friedrich-Alexander Universität in Erlangen, Germany
- 1995 Development Engineer for high-k Dielectrics and Oxygen Barriers at Siemens AG in Munich, Germany
- 1996-1997 Assignee for FeRAM Technology Development and Transfer at Symetrix Corp. in Colorado Springs, USA
- 1997 Start of PhD Thesis “Formation and Characterization of SrBi$_2$Ta$_2$O$_9$ (SBT) Thin Film Capacitor Module with Platinum/Titanium Bottom and Platinum Top Electrodes” under Prof. Dr. Waser at the Rheinisch-Westfälischen Technischen Hochschule in Aachen, Germany
- 1997-2001 Development Engineer for High Density FeRAM’s at Siemens AG (since 1999 Infineon AG) in Munich, Germany
- Since 2001 Integration Module Leader as Staff Engineer for 170nm and 110nm DRAM technologies at Infineon in Richmond, USA
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